The Last Barrier

Hammad M. Cheema and Atif Shamim

The last two decades have witnessed unprecedented development in the field of integrated circuits (ICs), driven by aggressive transistor scaling, unmatched levels of integration, advanced foundry processes, low cost, and improved yields. On one hand, digital integration, following the empirical prediction by Gordon Moore [1], has resulted in billions of transistors integrated in a few square millimeters, using processes that span the commercial range of 45 nm to 32 nm nodes [2] and transistors as small as 9 nm already demonstrated in research studies [3]. On the other hand, analog integration has also seen tremendous development (albeit at a relatively slower pace) resulting in highly integrated, multiband, multistandard transceivers for wireless communications [4]–[5].

Today's wireless systems comprise four major functionality-specific modules: the digital baseband module handling the signal processing, the mixed-signal module providing signal conditioning, the radio frequency (RF) front-end providing the RF carrier with modulated data, and the antenna for transmission of the signals. Traditionally, wireless systems have been developed by integrating these distinct functionality modules, either in a horizontal or a vertical fashion. This method offers the option of using the best technology for each component. For example, digital circuits are best suited to complementary metal-oxide semiconductor (CMOS) technology, power amplifiers may use III–V compound semiconductor technology, and antennas function efficiently on low-loss printed circuit boards (PCBs) such as FR-4, Duroid, etc. The horizontal integration results in the well-known multichip modules (MCMs) as shown in Figure 1(a) [6]. This approach consumes considerable chip area, which is a major disadvantage with the ever-reducing size of cellular and other wireless devices. Therefore, to reduce the form factors, the second approach of vertical integration using the system-in-package (SiP) approach, provides a useful alternative, as shown in Figure 1(b). Even in this case, the antennas, whose dimensions are on the order of wavelengths, still remain outside the package and usually are the largest components of the system [7]. Furthermore, integrating these different

Hammad M. Cheema (hammad.cheema@kaust.edu.sa) and Atif Shamim (atif.shamim@kaust.edu.sa) are with the IMPACT Lab, Electrical Engineering Department, King Abdullah University of Science and Technology (KAUST), Thuwal 23955-6900, Saudi Arabia. Hammad M. Cheema is also on leave from the School of Electrical Engineering and Computer Science, National University of Science and Technology, Islamabad, Pakistan.

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technologies becomes difficult, especially at higher frequencies, as the interconnects are lossy and the specialized processes such as flip-chip bonding increases the costs. Therefore, assisted by the advances in silicon technologies such as CMOS, the system-on-chip (SoC) approach has triggered significant interest, as it allows on-chip integration of digital baseband and complete RF front-ends, alleviating the need of transitions from one technology to another. At the same time, the application push toward the higher frequencies particularly millimeter-waves (mm-wave) at 60, 77, 94, and 140 GHz [8]–[13], has reduced antenna sizes to only a few millimeters, making it both possible and practical for on-chip implementation. There still exist a number of challenges for on-chip antennas: low antenna gains resulting from losses in low-resistivity silicon substrates; layout constraints due to metallization density rules and difficulties of on-wafer characterization, to name a few. Extensive research efforts are underway to overcome this final hurdle in achieving a true RF SoC solution.

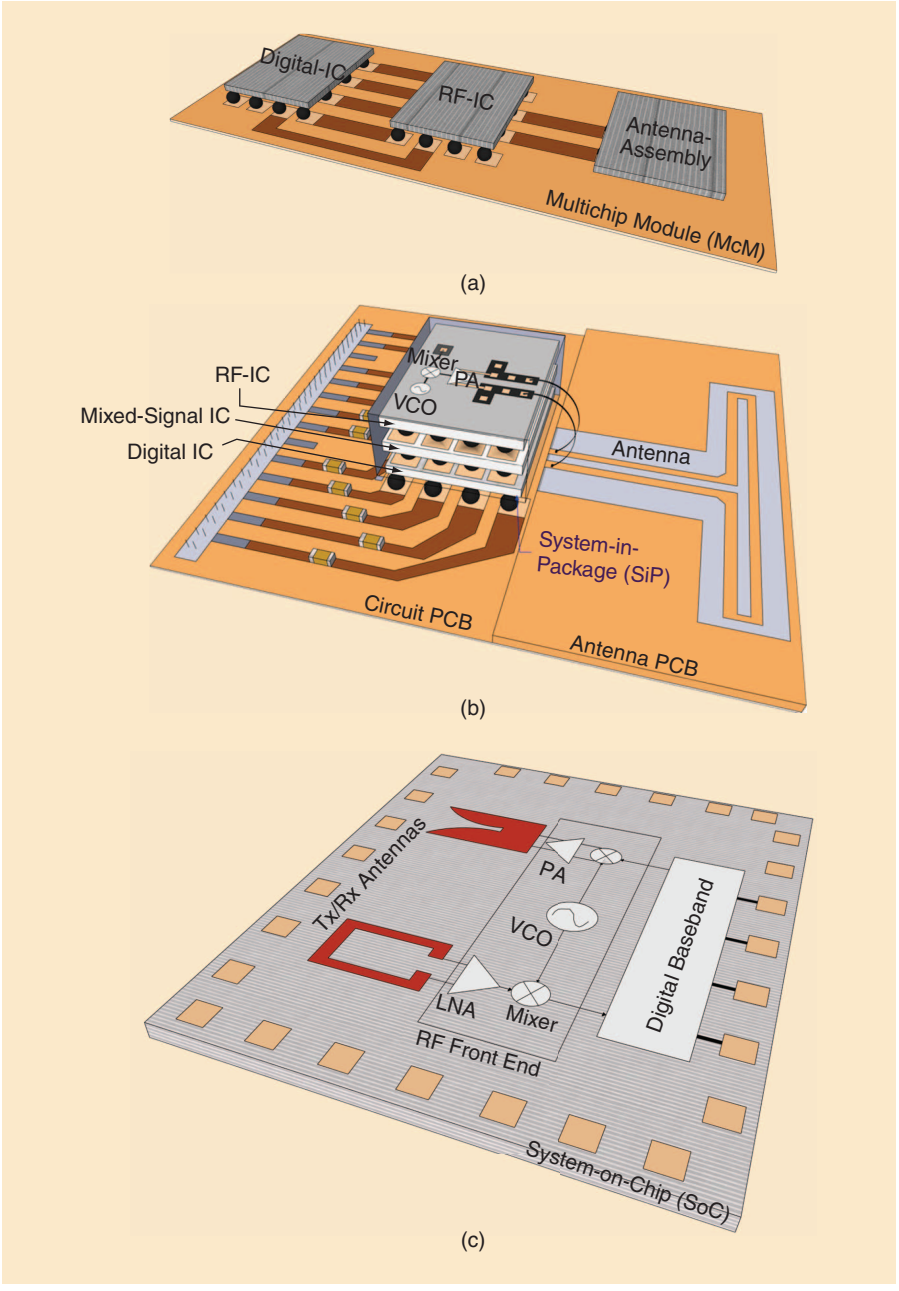

Figure 1. *Illustration of (a) an MCM, (b) an SiP, and (c) an SoC.*

On-Chip Antennas: Benefits and Challenges

50-Ω Boundary: Not Needed Anymore

The antenna, being the first component on the receiver (Rx) side and the last component on the transmitter (Tx) side, has to be interfaced to the electronic circuitry, whether in integrated or discrete fashion. Impedance matching is an essential requirement at the circuit-antenna interface to ensure maximum power transfer from one component to the other. As the circuit and antenna designers have traditionally remained isolated from each other during the design process, the famous 50-Ω impedance is pursued by both sides to achieve a matched condition [Figure 2(a)]. In doing so, the drawback is the need of matching elements to transform the complex impedances to 50 Ω. Furthermore, as antennas are conventionally implemented on PCBs, bond-wires are used to connect them to ICs. Consequently, the matching can be drastically affected, especially at higher frequencies, as these bond-wires are generally not well characterized.

In contrast, on-chip implementation of antennas can alleviate the above issues as the impedances of IC components [for example low-noise amplifier (LNA) on Rx and power amplifier on Tx side] need not to be matched to 50 Ω. Rather, codesign of antennas and circuits can ensure that their

complex impedances conjugately match each other without the need of a matching network [Figure 2(b)]. Using conjugate matching, the imaginary part of the two impedances has equal magnitude but opposite signs, thereby saving a number of extra components, space, cost, and design effort. The on-chip antenna also eliminates the uncertainty of bond-wires as metal interconnects directly interface the IC to the antenna feed point. The codesign and simulation for impedance matching between ICs and antennas together provides two degrees of freedom to the designer so that optimization can be achieved by leveraging the two domains between an LNA and receive antenna as in [14].

The above-mentioned codesign strategy is crucial for supporting the on-going trends of miniaturization for multifunctional, multistandard component integration and to understand the effects of circuits and antennas on each other. This implies that a new breed of designer is needed, one who understands both the IC and antenna worlds.

Silicon Substrate: Not Suited for On-Chip Antennas

The current semiconductor technologies are not equipped to support on-chip antennas. This is because the semiconducting substrates typically have a low resistivity of 10 Ω-cm, which is beneficial for ICs (as it avoids latch-up) but disastrous for on-chip antenna design [15]. For instance, a typical silicon based CMOS metal stack, shown in Figure 3, consists of six to nine metal layers placed in an oxide (SiO_2) that resides on top of a 500–600 μm thick substrate. The total thickness of the metal layers is around 15 μm with the top metal being the thickest (3–4 μm) and generally used to implement on-chip inductors. The antenna, which converts RF power from the circuits to electromagnetic (EM) radiation, finds a low-resistive path through the substrate and thus incurs gain degradation. The second drawback of implementing antenna in silicon based technologies is its high-dielectric constant ($\varepsilon_R \sim 11.7$), causing most of the power to be confined in the substrate instead of being radiated into free space, further degrading the radiation efficiency. According to [8], for a dipole antenna implemented on a silicon substrate, only 3% of the power radiates into the air and the rest is coupled into the substrate (Figure 4). Furthermore, the high ε_R and thick substrate results in surface waves which severely affect the antenna's radiation performance. This also means that Si substrate area around the antenna must be limited to minimize these surface waves. To counteract this surface-wave behavior, a number of techniques have been employed to improve the radiation efficiency of on-chip antennas by redirecting the power coupled into the substrate. One such solution is to incorporate an on-chip ground shield by utilizing one of the metal layers in the SiO_2 to isolate the lossy substrate from the antenna. But, as shown in Figure 3, the top and bottom metal layer distance in current IC technologies is approximately 15 μm, which does not provide enough separation between the antenna and the ground plane. This close proximity also causes image currents to flow in the ground plane with a subsequent loss of energy in the form of heat. This is also an issue for the antennas excited in a microstrip mode, as they cannot have a ground plane in the metal layers (at least below 100 GHz), whereas placing the ground plane at the bottom of the substrate means the EM fields will interfere with the ICs as well as get absorbed by the substrate, so generally coplanar waveguide (CPW) mode excitation is preferred for on-chip antennas. Another possible, albeit unconventional, way is to implement the antennas below the substrate, which would require through-silicon-vias (TSVs) to connect the antenna to the circuits above the substrate.

On-Chip Antenna Layout

The layout of silicon ICs is governed by a set of foundry-defined design rules. The design rules define, among other things, the maximum allowable widths of metal layers, the allowed spacings and the required metal densities on the chip. As antennas are typically not implemented on-chip, there are usually no specific rules or provisions for them in the foundry design rules. Consequently, it becomes difficult to resolve the design rule check (DRC) errors of the antenna layout. As an example, the maximum permissible width of the top metal layer is typically around 25 μm, which in many cases is not sufficient for on-chip antenna design. Such widths are required because larger metal widths offer low resistance, thus can handle more current resulting in higher EM radiation. This restriction

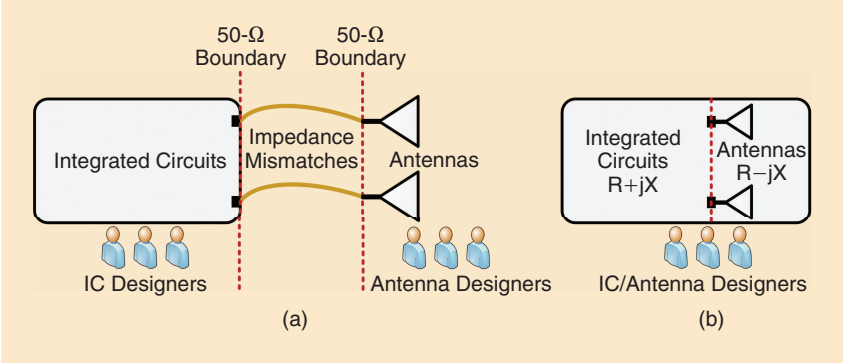

Figure 2. *(a) A traditional 50-Ω boundary between IC and antenna designers and (b) conjugate matching between IC and on-chip antennas.*

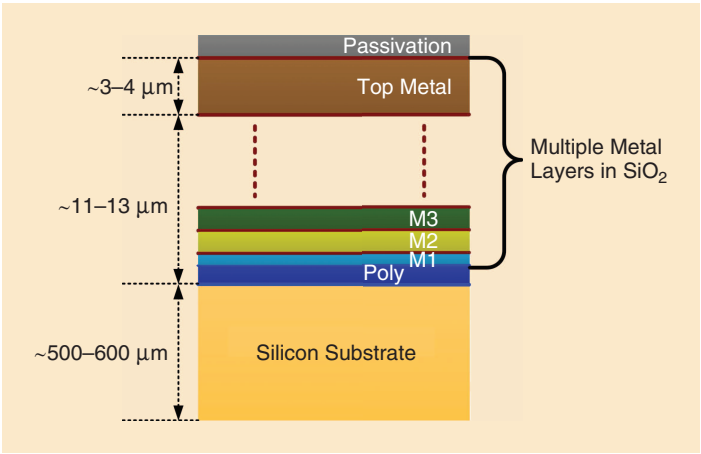

Figure 3. *A typical CMOS stack with multiple metal layers and a thick top metal for passive structures.*

on maximum width in most modern CMOS processes is to avoid electrostatic charge build-up at the transistors terminals which could potentially damage them. Similarly, the upper-limit on metal densities on the chip forces the on-chip antenna designer to subtract metal from the antenna, which might require reoptimization of the antenna. Fulfilling minimum metal density requirements for all metal layers, required for structural stability of the chip, imply that the final layout has to be filled with dummy metal blocks. None of this can be planned until the layout is near completion, as the final metal density is unknown in the initial design stages. The above difficulties require a number of iterations in the antenna design using EM tools then importing the design results into IC design tools and performing a DRC. Furthermore, until CMOS processes develop special rules for on-chip antennas, innovative solutions are required to accommodate DRC-error-free antennas in the layout. For instance, a work-around to overcome the electrostatic discharge (ESD) problem mentioned above is to provide a ground connection to the antenna in the top metal layer [16]. This ground connection will prevent destruction of the transistors due to ESD issues and can later be removed through microsurgery (lasering) to excite and characterize the antenna.

Parasitic coupling from the circuits to the on-chip antenna and vice versa is another layout issue. Today's highly integrated RFICs include many top-metal inductors, capacitors, bondpads, and transmission lines, which are usually placed in close proximity to save silicon area and to achieve short interconnects. It is important that circuit and bond pad placement with respect to antenna be carefully investigated in EM simulations. The placement of inductors is even more challenging as they also tend to radiate. A smart technique to layout close-by inductors is to ensure that currents in these inductors are in opposite direction with respect to the antenna, which cancels the radiated fields and reduces the mutual coupling as demonstrated in (Figure 5) [14]. Additionally, effects of nearby radiator element on circuits must also be assessed in post-layout circuit simulations. Unfortunately, no single simulation tool can handle such IC design as the on-chip antenna needs to be simulated in EM simulators like HFSS, whereas the circuit simulation and final layout has to be done in an IC circuit simulator like Cadence. In addition to minimizing the coupling through air, undesired coupling through the substrate must also be minimized. This can be achieved through guard rings around circuits and inductors. Compared to the on-chip circuits (typically hundreds of microns), the size of on-chip antennas is generally large (typically in millimeters) depending on frequency of operation. The ideal way to test antennas is to isolate them from the circuits and measure it as stand-alone structure. This means an identical antenna test structure has to be included in addition to the antenna integrated with the circuits costing valuable silicon area. Thus innovative layout techniques have to be adopted so that the same antenna that is integrated with circuits can be used for individual characterization as well. This might imply adding extra bondpads close to the antenna (Figure 6) or using the existing bondpads for multipurpose measurements.

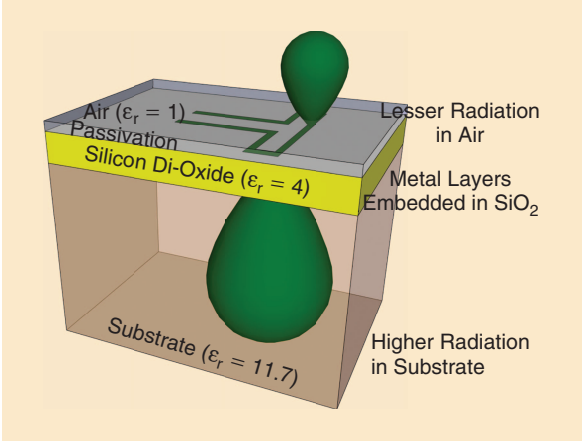

Figure 4. *EM radiation from on-chip antennas in silicon-based technology.*

On-Chip Antenna Characterization

The performance of fabricated on-chip antennas can deviate from the simulated ones for a number of reasons. For instance, the fabricated chips returned from foundries are generally polished from the backside, sometimes resulting in a different silicon substrate thickness than specified in foundry documentation. This discrepancy can not only change antenna impedance but also cause surface waves to change antenna gain and radiation pattern especially at mm-wave

frequencies. Similarly, interference or coupling from circuits on the same chip can affect the antenna performance. Thus, it is extremely important to characterize the antenna for its important parameters such as input impedance, gain and radiation pattern for these potential tolerances.

Antennas on conventional PCBs are typically characterized for their radiation pattern and gain characteristics by using transmit and receive towers in an anechoic chamber. This method is either not practical or prohibitive for measuring on-chip antennas due to the following difficulties. First, on-chip antennas are usually fed using small wafer probes, unlike the conventional coaxial or SMA feed mechanisms. The tips of the wafer probes land on bondpads and transmission lines are utilized to reach the actual feeding point of the on-chip antenna. These probe tips are very fragile and are likely to get damaged in case of movement of the antenna-under-test (AUT). Second, the large probe-arm holding the probes, independently or along with the probe-station, changes the AUT environment and may affect the measured results. Furthermore, the metallic chuck in the latter setup acts as a ground for the antennas and can yield unexpected measurement results, if not considered in design phase. Third, unlike conventional PCBs, silicon wafers are fragile and there is higher likelihood of wafer damage during measurements. This is because the wafer probes have to land on the bondpads, and a required over-travel is necessary for good contact. In some cases, this step lifts the metal from the wafer permanently damaging the bondpad. Fourth, a microscope is required to place the probes accurately on the miniature on-chip antennas or the lines feeding the antenna. Microscopes are not part of standard anechoic chamber equipment so it has to be judiciously placed in a way that does not affect the AUT radiation or block its movement. Finally, if the AUT is being measured in an anechoic chamber as opposed to a probe station, a special text fixture needs to be designed and fabricated in order to host the AUT. The impedance measurements are also carried out on the chip using wafer probes which need to be calibrated either using commercial impedance standard substrates (ISS) or custom calibration structures on the same wafer.

A number of innovative antenna characterization methods have been reported to address the above mentioned issues [16]–[21]. Most of these solutions focus on custom-made test fixtures for these nontraditional measurements. In [17], a compact probe-fed apparatus that employs a near field to far field transformation was used and includes a probe station, a fixed feed probe, a programmable scanning probe and a moveable microscope. The shielded circuit minimizes parasitic coupling and the scanning probe is capable of achieving a continuous scan in the selected range. In [19], an automated antenna measurement system was designed that utilizes a rotating conical antenna computer-controlled through a stepper motor. This system enables far field pattern measurement for a considerable range of angles. In [21], the interference in radiation generated by metallic objects of the probe station was countered by designing a custom-made rigid polyurethane carrier, which was attached to the probe positioner. This setup leaves almost all space around the AUT free of any metallic objects and allows a quasi-three-dimensional radiation pattern to be measured except behind the bottom of the probe. A custom-made test fixture is also shown in Figure 7 along with its usage at a probe station [22].

On-Chip Antennas State-of-the-Art Overview

There are four fundamental types of antennas that appear invariably as on-chip antennas. These are monopole, dipole, loop, and Yagi-Uda antennas. The choice of each is dependent on the requirements of gain, impedance, radiation, and the available chip area. Figure 8 shows a comparison between the four antenna types and their characteristics.

Having discussed the benefits and challenges of on-chip antennas, this section provides an overview of state-of-the-art in on-chip antennas in various semiconductor technologies. A majority of the on-chip antennas in the last few years have been implemented in bulk silicon- (with low resistivity of 10 Ω-cm) based technologies such as CMOS and SiGe as opposed to other semiconductor technologies (with high resistivity) such as GaAs. This trend is expected as CMOS

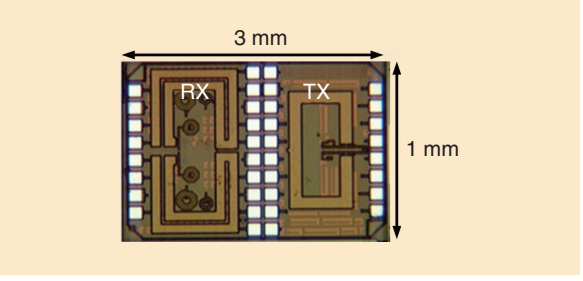

Figure 5. *Close proximity of inductors, transmission lines, and circuits to on-chip antennas [22].*

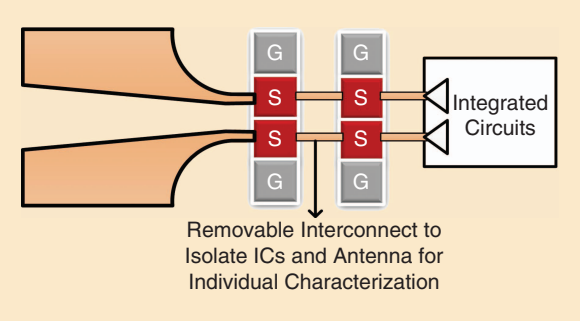

Figure 6. *An example layout for characterizing an integrated antenna after isolating it from the ICs.*

has become the mainstream choice for IC designs and extensive investigations to bring the elusive antenna on-the-chip have been carried out.

Traditionally, GaAs based bipolar technologies had the reputation as a high-performance technology, especially at high RF frequencies, and for providing power amplifiers with high output powers. This was possible as bipolar transistors employed vertical current transport, which led to the higher power density. In addition, GaAs substrates were semi-insulating with high resistivity that was beneficial for on-chip antenna implementation. Silicon-based technologies, especially CMOS, through continuous down-scaling, have demonstrated improved unity current gain frequency (fT) and unity power gain frequencies (f_{max}). CMOS also supports a high level of integration, offers improved process options and lower costs for mass production. Furthermore, in comparison to two or three metal layers offered in GaAs, six to nine metal layers are available in CMOS processes, adding flexibility for on-chip antennas. The substrate however, still remains the main problem due to its low resistivity.

The following overview of on-chip antennas is divided in two categories: bulk silicon based having low-resistivity substrates (CMOS and SiGe) and other technologies including GaAs and specialized high-resistivity processes.

Complementary Metal Oxide Semiconductor (CMOS) and Silicon Germanium (SiGe)

Table 1 lists some of the state-of-the-art CMOS and SiGe on-chip antennas. The information in the table shows that more focus is on on-chip antennas with transceivers [24], [26], [29], [30] and other on-chip components rather than stand-alone antennas. The majority of the reported antennas have been implemented in 0.18 μm and 0.13 μm CMOS processes apart from [24] which uses 65 nm. As a result of the small footprint required, most of the antennas in Table 1 are operating at millimeter wave frequencies such as 60, 90, and 140 GHz. There are few exceptions for antennas operating at frequencies lower than 10 GHz [26], [29]. In [17], a differential antenna integrated with an on-chip balun is discussed. Differential antennas are easy to combine with differential circuits, which are preferred by IC designers because of their noise immunity. A balun is then required so that typical single-ended network analyzers may be used for measurements. De-embedding the balun is required to observe the antenna performance. Many designs shown in Table 1 are either not characterized independently or their radiation patterns are not reported, mainly because the integrated antennas are measured on-wafer using probe-stations and it is therefore challenging to incorporate conventional antenna characterization techniques and innovative workarounds have to be used as discussed earlier. Standard CMOS on-chip antennas typically exhibit low gains. For example, the loop and dipole antennas in [22] have gains of –22 and –35 dBi (dBi is used to express the gain of an antenna in decibles relative to the gain of an isotropic antenna). Similarly, the multiturn dipole in [26] demonstrates a –30 dBi gain. One exception is the linear tapered slot rectenna reported in [28] which has positive gains of 7.4 and 6.5 dBi at 35 and 94 GHz, respectively. The size of this slot rectenna, 1×2.9 mm^2 is considerably larger than the other designs, and, more importantly, the resistivity of the substrate is unknown and it might have been implemented in a high-resistivity process. At millimeter-wave frequencies, the antenna sizes are inherently smaller due to smaller wavelength. Therefore, the real challenge in reducing on-chip antenna sizes is faced at lower frequencies where the architecture choices and miniaturization techniques must be applied. For instance, previous studies demonstrate a 5.2 GHz loop antenna only occupying 0.82×0.67 mm^2, thus avoiding a silicon area penalty [29]. Miniaturization techniques will be discussed in the next section.

On-chip antennas have also featured regularly is the SiGe heterostructure bipolar transistor (HBT) technology, some of which

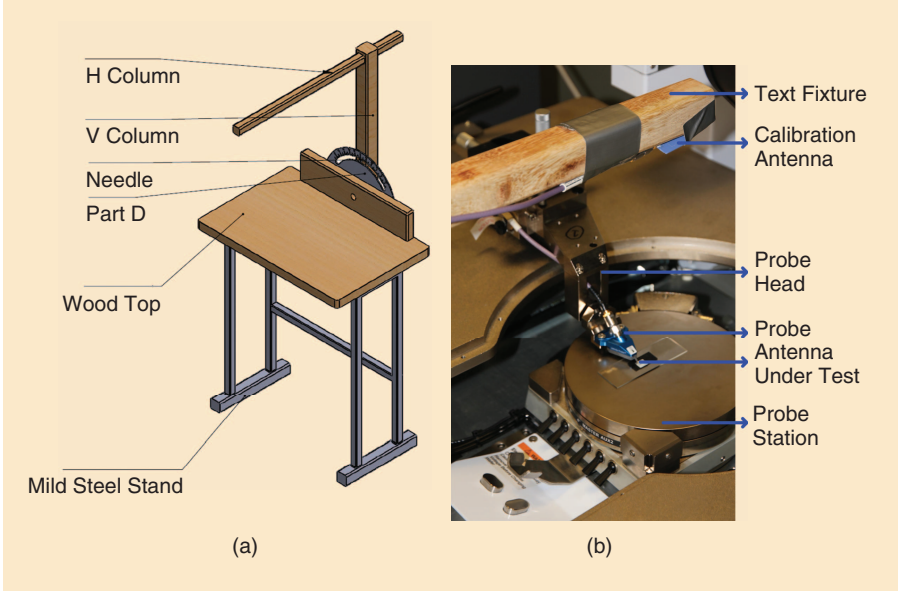

Figure 7. *(a) A custom text fixture and (b) RF probe feeding the on-chip antenna [22].*

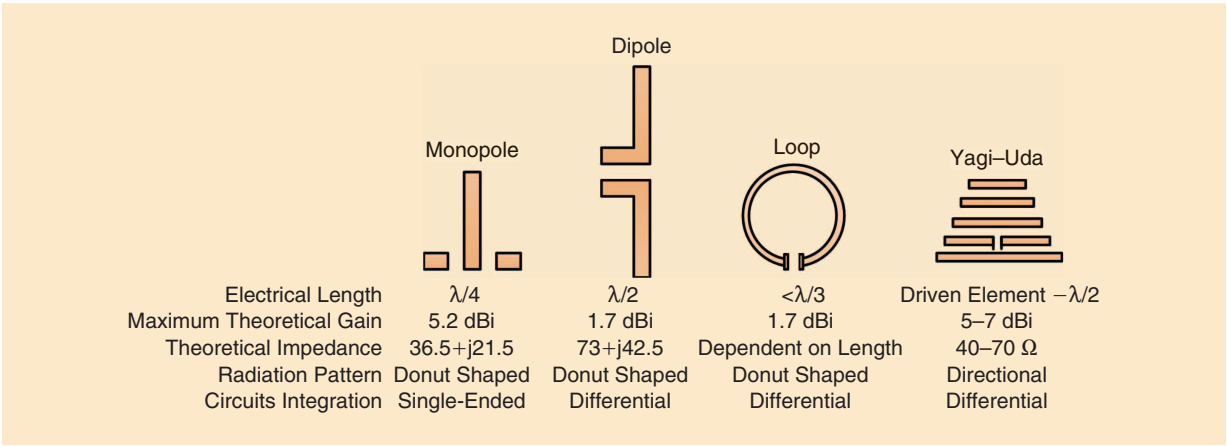

Figure 8. *Four fundamental antenna types and their characteristics.*

are mentioned in Table 1 [8], [37]–[39]. Apart from [39], the rest of the antennas operate at 77 GHz, 94 GHz, or higher frequencies with simple dipole and patch being reported. The antenna gain on standard SiGe process in [37] is −10 dBi. However, using a quartz substrate on top of the metal stack improves the gain, as a 3.9 dBi gain shown in [38]. Similarly, a dielectric resonator (DR) used on top of SiGe results in a high gain of 0.5 dBi in [39] and a backside lens used in [8] yields a gain of 2 dBi.

Other Technologies—GaAs, High-Resistivity and Specialized Processes

Table 2 lists a number of on-chip antennas implemented in GaAs technology [31]–[35], showing various antenna architectures including dipole, log periodic, patch and slot antennas. The majority of the designs target mm-wave frequencies, including the 60 and 94 GHz bands, and due to the difficulty in characterizing on-chip antennas at these frequencies, gain and radiation patterns are not shown for most designs. A typical two-metal-layer stack up of GaAs technology used in [55] is shown in Figure 9. The GaAs wafers have a high resistivity of the order of 10^7 Ω-cm, with subsequently lower losses, resulting in higher antenna gains as reported in [33], [35]. The dielectric constant of 12.9 is similar to silicon; but, in contrast to surface waves issue in slightly thicker silicon substrates (300–700 μm), thinning the GaAs substrate to 100 μm as in [33], [35] reduces the surface waves and enhances the radiation efficiency. The reported antenna sizes in Table 2 occupy a few square millimeters of chip area.

In [36], a folded dipole implemented in a high-resistivity SiGe technology and integrated with a 24 GHz Rx demonstrates a –2 dBi gain which is higher as compared to antennas implemented in a low-resistivity Silicon SiGe process, for example [37]. Table 2 also lists on-chip antennas implemented in specialized processes offering high-resistivity substrates, artificial magnetic conductors (AMC) and high-impedance layers [40]–[43]. Silicon-on-insulator (SOI) CMOS has been used in [41], alleviating the disadvantages of lossy silicon substrate by placing a thin Si layer on an insulating oxide substrate such as sapphire. The design targets 60 GHz with a gain of 3.9 dBi. In [42], a high-impedance surface (HIS) is itself used as an antenna using arrayed dog-bones over a ground plane demonstrating a gain of 5 dBi at 6 GHz. The antennas in [40]–[43] show higher gains compared to antennas implemented in standard technologies. Since these special processes are not mainstream and involve multiple post-processing steps, the complexity and relevant costs are higher.

New Trends in On-Chip Antennas

The advantages of on-chip antennas as discussed in preceding sections has led to their consideration for emerging areas such as THz, biomedical, MEMS, and energy harvesting applications. At the same time, advanced techniques for miniaturization and efficiency enhancement for on-chip antennas are being investigated. This section summarizes these new trends.

Terahertz Antennas

The spectrum between 300 GHz and 3 THz is broadly referred as the THz band. This band can be used for detection of chemicals, for imaging of concealed weapons, cancer cells and manufacturing defects, and for short range radars, and secure high-data-rate communications [56]–[57]. The improvement in high-frequency performance of silicon based technologies has made it possible to consider them as a lower cost alternative to III-V technologies and explore the THz band for various applications [44]–[46]. A THz spectrometer for chemical detection has been presented in [44] which integrates patch antennas both on the Tx side with the signal generator and on the receive side with a Schottky diode mixer. In [45], a 650 GHz SiGe Rx for THz imaging arrays uses an on-chip folded dipole antenna and simultaneously provides a low-loss path for the common mode to act as a RF-LO combiner. The simulated gain of the antenna is −2 dBi at 650 GHz.

TABLE 1. State-of-the-art on-chip antennas in low resistivity bulk silicon technology.

Reference	Process	Architecture	Frequency (GHz)	–10 dB Bandwidth (GHz)	Gain (dBi)	Chip Area (mm x mm)	Comments
[17]	Bulk silicon wafer	Conductor-backed dipole	24	20–30	–8	0.5 × 3	Antenna integrated with balun, near field radiation pattern measurements
[19]	0.18-μm CMOS	Yagi, dipole rhombic, loop	60	53–65, 54–65, N/A, N/A	–3.5, –7.3, –1.2, –3.4	1.2 × 0.05, 1.2 × 0.03, 5 × 5, 5 × 5	Performance at various chip locations studied, new measurement setup
[23]	Post-BEOL CMOS	Inverted-F and Quasi Yagi	60, 65	55–67.5, 0	–19, –12.5	0.2 × 2, 0.4 × 1.3	First on-chip antennas for 60-GHz radios, two-antenna method for gain measurement
[24]	65-nm CMOS	Dipole	28	N/A	N/A	0.04 × 1.58	Integrated with Tx, rectangular silicon lens used to increase gain by 8–13 dB
[25]	0.18-μm CMOS	Yagi	60	55–65	–9	1.1 × 0.95	Director and reflector to improve gain
[26]	0.18-μm CMOS	Multiturn dipole	5.8	5.7–5.8	–29.8	N/A	Integrated with rectifier for power scavenging
[27]	Standard CMOS process	Cavity-backed slot antenna	140	135–141	–2	0.6 × 1.2	One of the highest operating frequencies in standard CMOS, comparison between HFSS and CST
[28]	0.13-μm CMOS	Linear tapered slot antenna	35, 94	25–65, 75–105	7.4, 6.5	1 × 2.9	Highest reported gains, two-antenna method used for radiation pattern measurement
[29]	0.13-μm CMOS	Loop	5.2	N/A	–22	0.67 × 0.82	Loop antenna used as VCO inductor
[30]	0.13-μm CMOS	Slot	9	N/A	–4.4	0.55 × 0.55	Gain enhanced through image current cancellation, lower metals used as ground shield
[8]	0.13-μm SiGe BiCMOS	Dipole	77	N/A	2	0.004 × 0.02 × 1.15	Integrated with Rx , backside lens increases gain by 10 dB
[37]	0.13-μm SiGe HBT	Dipole	160	N/A	–10	0.45 × 0.5	Wafer probes used for indirect gain measurement
[38]	Quartz substrate on top of SiGe BiCMOS	Microstrip patch	94	91.5–98.5	0.7–3.9	0.97 × 0.69	125-μm-thick quartz substrate placed on top of silicon stack to improve gain
[39]	DR on top of SiGe	H-slot	35	33–37	0.5	1 × 1.15	Adding DR and removing passivation between H-slot and DR improves radiation efficiency

A 2.2 × 1.9 mm^2 SiGe frequency modulated continuous wave (FMCW) radar transceiver chip reported in [46] operates at 0.38 THz. The Tx includes two oppositely directed patch antennas and has simulated gain of 6.3 dBi. Similarly, the Rx contains two patch antennas and utilizes a ground plane to isolate signals from the silicon substrate and prevent surface-wave excitation. The simulated gain of the receive antennas is 6.6 dBi. There are a number of challenges in the design of on-chip THz antennas. For example, special

TABLE 2. State-of-the-art on-chip antennas in technologies other than low resistivity bulk silicon.

Reference	Process	Architecture	Frequency (GHz)	−10 dB Bandwidth (GHz)	Gain (dBi)	Chip Area (mm x mm)	Comments
[31]	0.15-μm GaAs	Folded slot	60	59–65	N/A	1.25 × 1	Active antenna integrated with Rx
[32]	GaAs	Planar dipole	18	12–24	N/A	3 × 0.21	Direct integration with Schottky diode
[33]	Thin GaAs substrate	Log periodic	94	87–99.5	4.8	1.2 × 2.6	Substrate thinned from 700 to 100 μm using lapping process
[34]	GaAs	Slot substrate Integrated waveguides	60	58.5–61.5	N/A	1.34 × 0.04	Active antenna integrated with MCM Rx
[35]	GaAs	Dual band patch	57, 59	57–57.7, 59–59.5	1.5, 1	1.25 × 1	Integrated with BPSK Tx, substrate thinned to 0.1 mm
[36]	0.8-μm SiGe HBT	Folded dipole	24	N/A	−2	2.1 × 0.6	High-res. substrate, integrated with LNA, LO, and mixer
[40]	90-nm CMOS	AMC embedded squared slot antenna	60	15–66	2	1.44 × 1.10	AMC removes image current, etched ground plane used
[41]	SOI CMOS	Folded slot	60	53–64	3.9	0.8 × 1.7	New measurement setup for gain and radiation pattern
[42]	High-impedance substrate	Arrayed dog bones as magnetic resonator	6	5–8	5	3.5 × 0.875	HIS used as antenna itself
[43]	CMOS with HIL	Dipole with HIL below	90	85–97	1.2	2 × 1.2	HIL used as both AMC and radiating element

fabrication techniques such as electron beam lithography is required to manufacture the nanoscale structures. Secondly, the low efficiencies of on-chip antennas at THz frequencies have to be addressed, and finally, the characterization of these structures cannot use probe-fed methods as the probes are much larger than the antenna structures. Therefore, indirect measurements using coupling methods might be adopted.

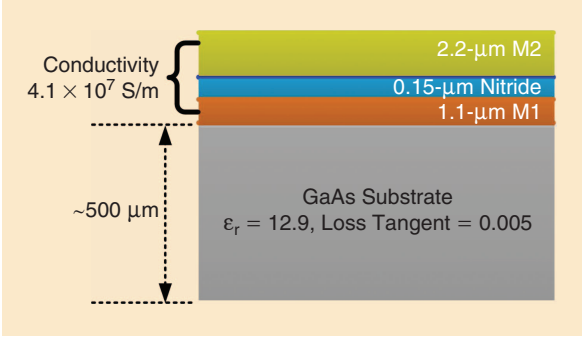

Figure 9. *A typical two-metal layer stack up of GaAs technology with semi-insulating substrate.*

Efficiency Enhancement of On-Chip Antennas

Efficiency and gain of on-chip antennas have been improved by using high-resistivity substrates such as SOI [41]. As these processes are not as mainstream as bulk CMOS, alternative methods to achieve the same performance in standard bulk silicon have been sought by researchers. For instance, in [8] a silicon lens is used at the back of the chip and the bulk silicon substrate is convex-shaped to ensure that the wave is constructively enhanced at the backside of the chip. This post-processing method boosts the gain by 10 dB at 77 GHz. The second method of enhancing the antenna efficiency is the use of an AMC. A ground plane at the bottom of the silicon substrate induces oppositely charged image current that destructively interferes with the antenna currents. The AMC isolates the ground plane by inducing image currents in its own surface, constructively interfering with the antenna currents and boosting the antenna efficiency. Taking advantage of the multiple metal layers in today's silicon technologies, AMCs can be implemented without any cost or post-processing penalties (Figure 10). In

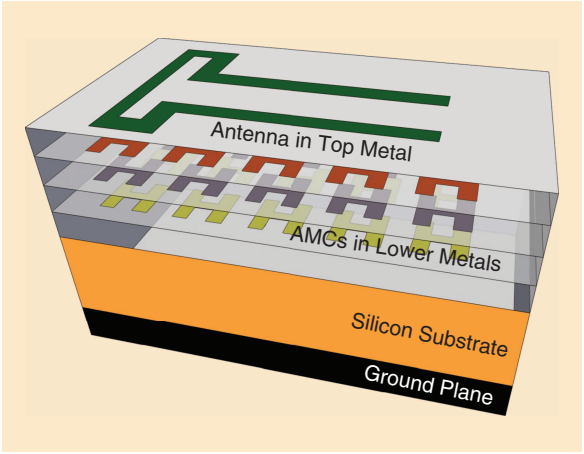

Figure 10. *Use of AMCs to enhance on-chip antenna efficiencies.*

[40], AMCs are embedded by forming an array of two opposite faced structures resembling English alphabet Cs and replicating them from metal layer 1 to metal layer 5, with the squared antenna fabricated in metal layer 6. This method provides a 9 dB gain improvement and yields a 2 dBi gain and a wide bandwidth of 15–66 GHz. A similar concept is used in [43], where a high-impedance layer (HIL) composed of dog-bone shaped conductors is implemented in metal layer 5 whereas a dipole antenna is present on metal layer 6. The HIL, while operating close to its magnetic resonance value, acts as an AMC. The reported gain of the dipole antenna at 94 GHz is 1.2 dBi

Miniaturization of Low Frequency On-Chip Antennas

The antenna designs shown in Tables 1 and 2, apart from a few low-frequency designs, list on-chip antennas that target millimeter wave frequencies as the footprint at these frequencies is small, and thus affordable and manageable for on-chip implementations. The challenge for on-chip antenna designers is to find ways to miniaturize these antennas at low frequencies. Many miniaturization techniques have been discussed in [47] for antennas implemented on conventional RF boards. Some of these techniques can also be adopted for on-chip antennas. For instance, slot loading involves cutting off metal slots from a planar patch antenna, thereby forcing a longer path for the current, and reducing the resonant frequency of the patch. Another technique is to use meandering, in which a straight antenna path is reshaped to a continuous periodically folded structure, resulting in a lower resonant frequency for the same antenna footprint. This is shown in [48], where a planar inverted-F antenna (PIFA) reduces the area by more than 30% in comparison to a nonmeandered antenna (Figure 11).

A third potential miniaturization technique for on-chip antennas is using fractal geometries. Fractal geometries are formed in an iterative manner by repeating and scaling of unique shapes within a given footprint. Fractal antennas exhibit multiple resonances and may be suitable for wideband applications.

Another miniaturization technique involves slow-wave structures that offer immense potential for miniaturization of on-chip antennas as they are quite suitable for on-chip implementation. The dimensions of an antenna are related to the phase velocity $\lambda = v/f$, implying that if the phase velocity (v) can be reduced, the antenna size could be reduced for the same frequency of operation, or alternatively, keeping the antenna size constant a lower frequency of operation can be achieved. The phase velocity is also related to the inductance and capacitance of the antenna structure ($v = 1/\sqrt{LC}$) which provides a rather simple way of manipulating the phase velocity by adjusting the L and C values. Slow wave structures including shunt capacitors and/or series inductors can be implemented on-chip by modifying the structure of the antennas. Typical resonant antennas (such as the $\lambda/2$ dipole) yield 73 Ω impedance (which can be matched to 50 Ω by varying the feed-point). Alternatively, this impedance can also be achieved by reducing the electrical length of the antenna (hence miniaturization) and compensating the impedance mismatch through matching elements. Despite the use of these techniques, there are still not many low frequency on-chip antennas (below 5 GHz) that have been published in literature for typical chip sizes of few millimeters. This is still an active area of research.

MEMS Antennas Codesign with CMOS

In the last decade, MEMS have come of age and a number of components, which exhibited performance limitations in conventional silicon processes, have demonstrated improved performance in MEMS. For instance, MEMS is readily used for switches with low insertion loss, for tunable resonators and filters, and for variable capacitors and inductors. MEMS can provide tunability and reconfigurability by physical movement of the structures, either by the application of actuation voltages or by other mechanisms. MEMS has been used to design switchable and reconfigurable antennas at various frequencies. In [49], a slot-array antenna is reconfigured by switching each slot individually through MEMS, thereby achieving beam steering. Efforts are also underway to integrate the MEMS structures with on-chip RFICs to obtain the best of both worlds [50]. Major post-processing steps such as dry and wet etching, are required to achieve such integration. These major post-processing steps for CMOS-MEMS integration have hindered its mass appeal. Therefore, the inclusion of MEMS in standard CMOS processes is still an active research area and IC foundries are investigating the potential for a mainstream CMOS-MEMS process. For on-chip antennas, the possibility of using MEMS will be highly beneficial as the antennas could potentially be suspended in air and

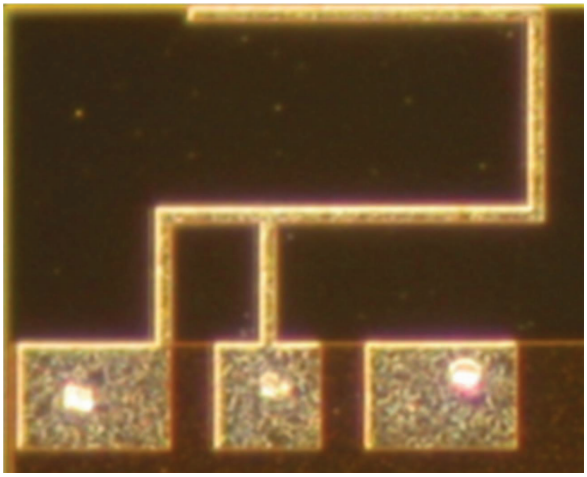

Figure 11. *Planar inverted-F antenna meandering reduces more than 30% chip area [48].*

away from the silicon substrate (Figure 12). Thus, all the disadvantages associated with low resistivity and high-permittivity of the silicon substrate can be minimized to improve on-chip antenna gains and efficiencies.

On-Chip Antennas for Intra- and Interchip Communication

Wired interconnects used for connecting components in CMOS technology degrade the system performance through the associated parasitics. The increase in operating frequency of modern communication systems and decrease in feature size result in smaller line widths and spacing between these interconnects, further affecting their performance through enhanced inductive, resistive and capacitive coupling [14]. These issues of wired interconnects can be reduced by using on-chip antennas which communicate electromagnetically instead of electrically between the different components (Figure 13). The mode of communication can be either intrachip (on the same chip) or interchip (between different chips), depending on the targeted application. For example, clock distribution in SoC implementations can benefit from wireless intrachip communication [51], whereas vertically integrated chips in SiP or system-on-package (SoP) can employ wireless interchip communication [52]. Thus, the wireless interconnect concept can help reduce the complexity of highly integrated systems.

Implantable Antennas

In the newly emerging body-centric communications paradigm, on-chip antennas can be used as implantable devices for military, medical and commercial applications. For medical implantations, the size of the system should be small. The typical frequencies employed for such systems being in MHz and low GHz range makes the corresponding antenna comparatively large. If these antennas can be implemented on-chip, miniaturization of the implantable system can be achieved. Some examples, such as implanted antennas for biomedical therapy and diagnostics, have been designed to produce hyperthermia for treating tumors and monitor various physiological parameters [53]. Furthermore, on-chip antennas in conjunction with various kinds of sensors can be implanted as part of a biotelemetry system in order to establish wireless communication between implantable devices and exterior instruments. In such an implementation, the implanted antenna can be used for on-chip energy harvesting to both operate the circuits as well as establish communication with the outside world. Modeling of implanted antennas in various parts of human body and creating a testing environment for fabricated structures are some of the challenges being addressed by researchers.

Nano-Electromagnetic Collectors

The EM radiation emanating from the sun provides a constant source of energy to the earth. Approximately 30% of this energy is reflected back to space, 19% is absorbed by atmospheric gases and re-radiated to the earth's surface in the mid-infrared range (7–14 μm), and 51% is absorbed by the earth's surface and organic life and re-radiated around 10 μm infrared wavelength [54]. Modern lithographic techniques allow realization of on-chip nanoantennas [also called nano-EM collectors (NEC) or nantennas] that can resonate in the infrared frequency range to capture EM energy and convert

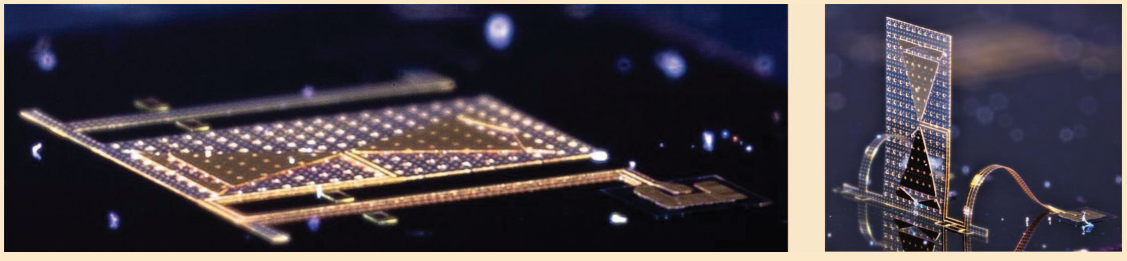

Figure 12. *MEMS antenna on silicon substrate: (a) in horizontal position and (b) in vertical position [58].*

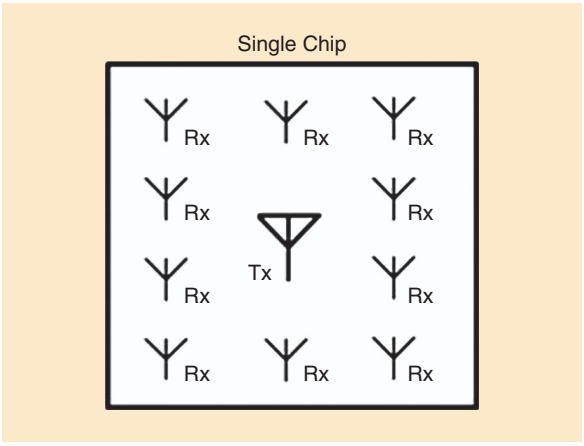

Figure 13. *A wireless interconnect illustration for intrachip communication.*

it into useful source of electricity. Similarly, they can also be configured to capture energy from the visible part of the frequency spectrum. As these antennas rely on natural resonance and bandwidth of operation is dependent on physical dimensions, they are found to be more efficient than conventional photovoltaics [54]. NECs offer immense potential as huge panels having millions of on-chip nantennas can be placed on roofs, windows etc. The nanoscale rectifiers, which are required to convert the captured EM energy, to usable electricity, still remain an elusive challenge for researchers.

Conclusions

This paper has presented a comprehensive overview of on-chip antennas, which remain the last bottleneck for achieving true SoC RF solutions. CMOS remains the mainstream IC technology choice but is not well suited for on-chip antennas, requiring the use of innovative design techniques to overcome its shortcomings. Codesign of circuits and antennas provide leverage to the designer to achieve optimum performance. The layout of on-chip antennas is dictated by foundry specific rules whereas characterization of on-chip antennas requires special text fixtures. For future highly integrated SoC solutions, foundries will have to provide special layers for efficient on-chip antenna implementations, as they currently do for on-chip inductors. In many of the emerging applications such as THz communication, implantable systems and energy harvesting, on-chip antennas have shown immense potential and are likely to play a major role in shaping up future communication systems.

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