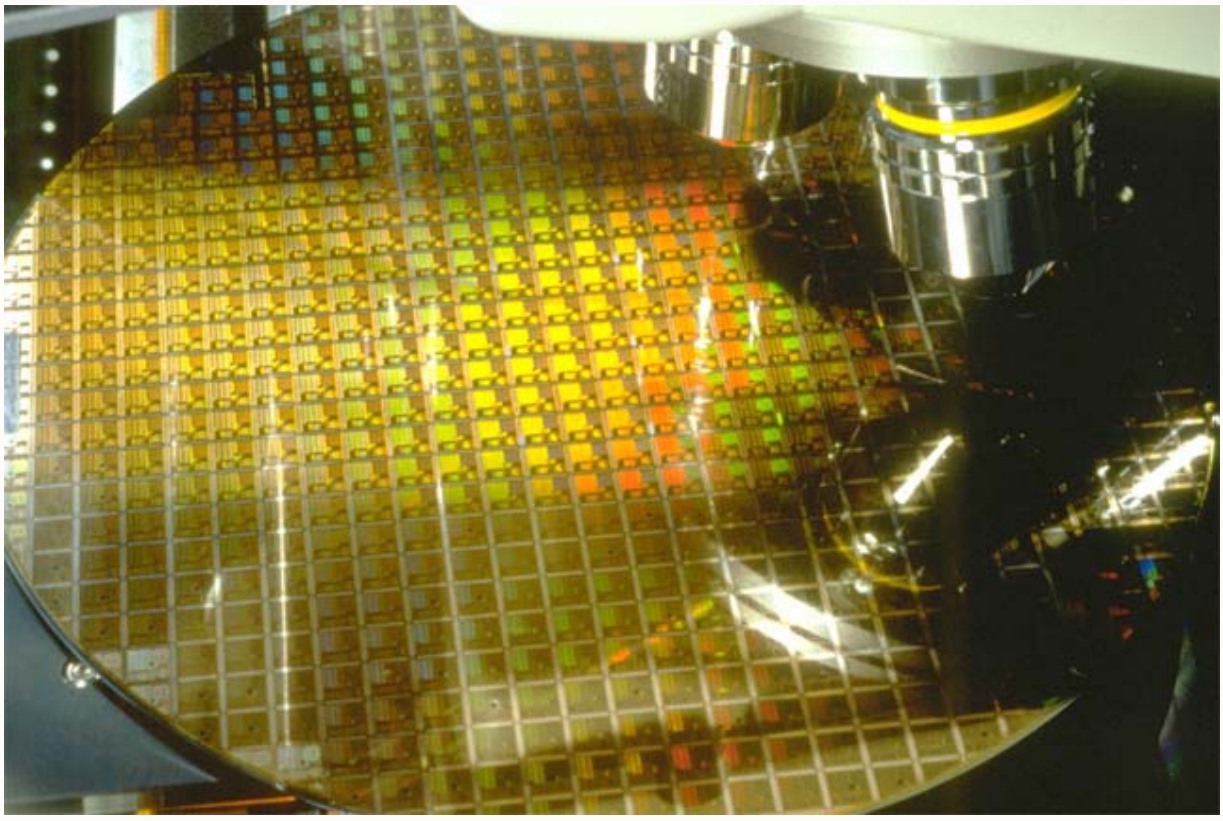
CMOS/Processing technology



Source: TSMC

CMOS/Processing technology

- Why MOS/CMOS?
  Dimensions of MOS devices can be scaled down more easily than other transistor types
- Starting mid 1960's: Shift from NMOS to CMOS
  Main reason: "Zero" static power dissipation
- CMOS technology was attractive because of the relative small number of masks (about 7)
- Modern CMOS processes:
  - about 200 process steps
  - about 25 masks
    Number of masks heavily impacts unit price of the chip. Each mask costs n*$1k (total mask cost typ. $200k). Lithography is slow.
  - up to 6 (and sometimes more) metal layers
  - Poly layers: 1 (standard) or 2 (non-standard, e.g. E^2prom)
  - Today's standard: n-well CMOS process with self-aligned polysilicon gates

CMOS/Process steps

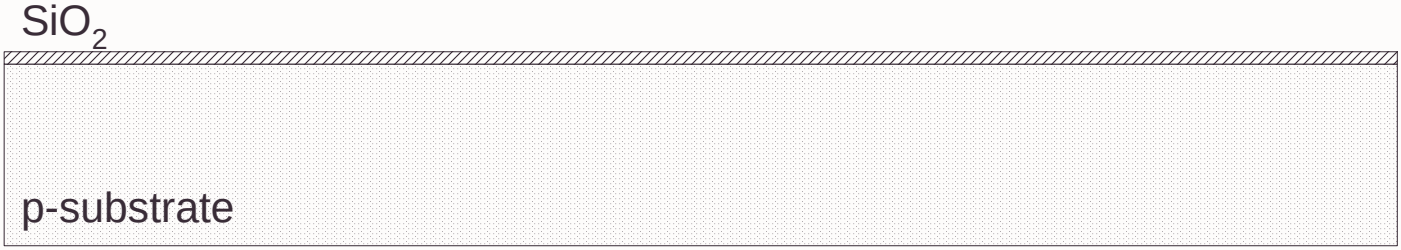
– Process step: Wafer fabrication

- Czochralksi method:
  - Seed of crystalline Si is immersed in molten amorphous Si (1425°C). Molten Si contains desired level of p-type doping.
  - Seed is gradually pulled out while rotating (30-180mm/h)
  - Result: Large single-crystal cylindrical ingot
- Ingot is sliced into thin wafers
  - Wafer sheet resistance: 50-100mΩ
  - Initial wafer thickness: 500-1000μm
  - Wafer diameter: 75-300mm (12 inch)
- Wafers are polished and etched to remove surface damages

CMOS/Process steps

– Process step: Grow thin layer of SiO_2 on p-type wafer

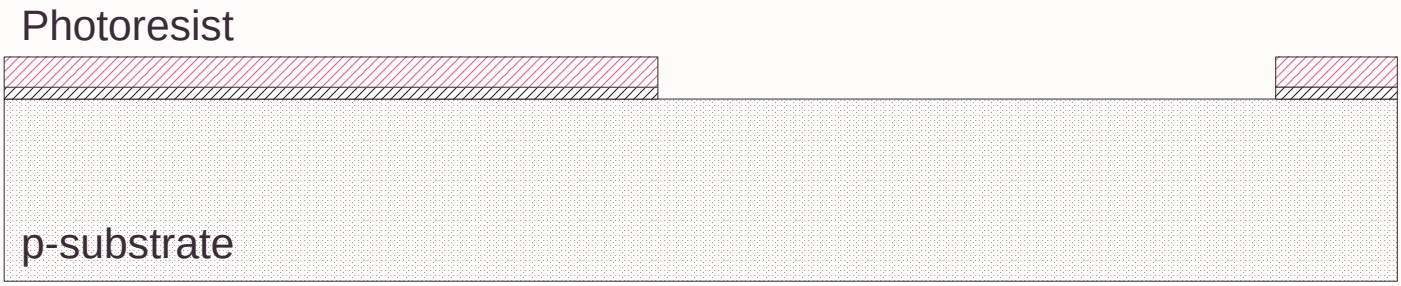
- Place wafer in an oxidizing atmosphere at around 1000°C
- Unique property of Si: a very uniform oxide layer can be produced on the surface with little strain in the lattice
- Oxide layers can be very thin (e.g. 50Å=5nm), only a couple of atomic layers
- Oxide can be used as gate dielectric (TOX). Oxide can also grown thick (field oxide FOX) as a foundation for interconnect lines
- Oxide also serves as a protective coating during many process steps (like in this process step)



CMOS/Process steps

– Process step: Lithography sequence for n-well

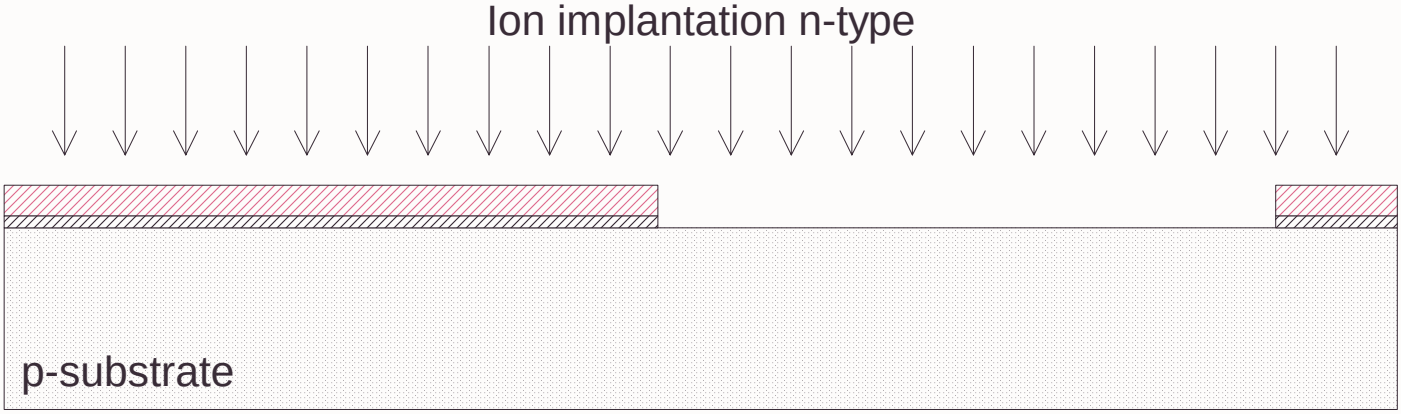
- Photolithography: Transfer circuit layout information to the wafer
  Layout consists of polygons. Layout is first “written” to a transparant glass “mask” by a precisely controlled electron beam.
- Negative Photoresist (PR) deposition
  PR: A material whose etching properties change upon exposure to light. Negative PR “hardens” in regions exposed to UV light. Positive PR “hardens” in regions not exposed to UV light.
- Exposure to ultraviolet (UV) light using the n-well mask
- Selective etching. Etchant dissolves “soft” PR



CMOS/Process steps

– Process step: Create n-wells through ion implantation

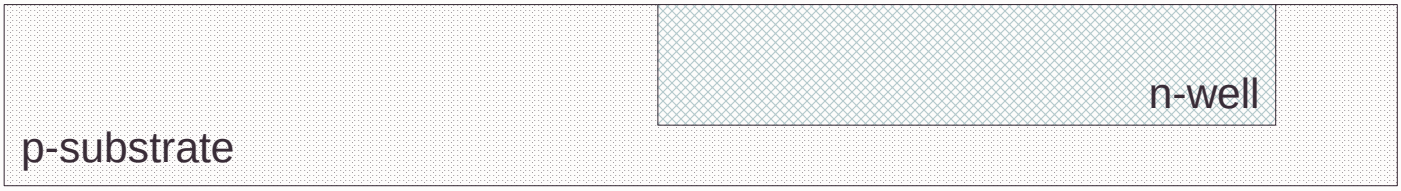
- n-wells required for p-channel devices
  n-channel devices will be fabricated directly in the native p-substrate
- Ion implantation: Selectively introduce dopants into the wafer
  Doping atoms are accelerated as a high-energy focused beam, hitting the surface and penetrating the exposed areas. Doping level determined by intensity and duration of implantation.
  Retrograde profile: Peak of the doping concentration occurs well below the surface



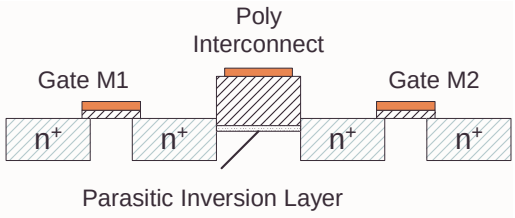
CMOS/Process steps

– Process step: Remove PR and oxide layer

- n-well completed
- Note: Ion implantation damages the Si lattice
  Si lattice can be repaired through an annealing process. Annealing: Wafer is heated to 1000°C for 15-30min allowing the lattice bonds to form again. Annealing causes dopant diffusion in all directions (e.g. side diffusion of S/D regions). Therefore, wafer is annealed only once after all implantations have been completed

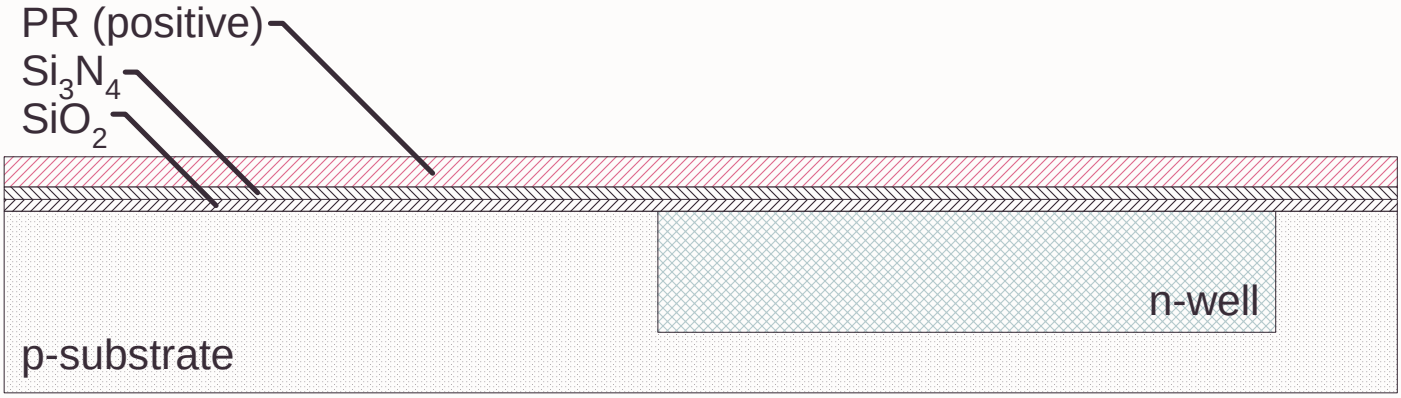


CMOS/Process steps



– Process step: Channel-stop implant (1)

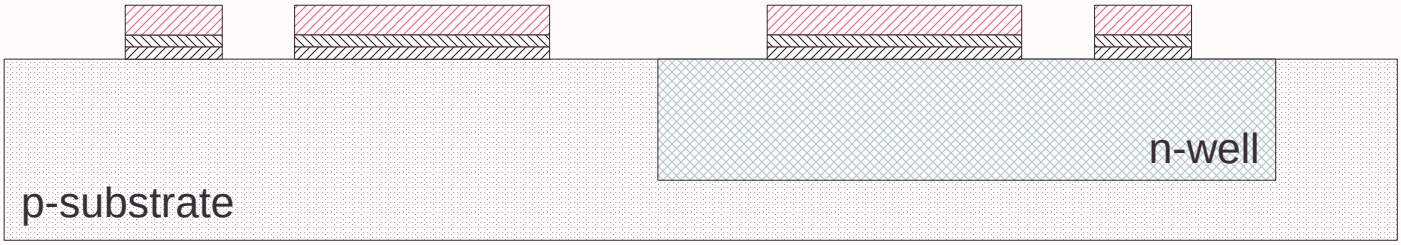
- Channel-stop implant required to prevent parasitic mosfets
  Prevents conduction between unrelated transistor sources and drains (and wells). Two n+ regions and the FOX from a transistor. FOX is thick, therefore transistor has a large Vth. Nonetheless, a sufficiently positive potential on the interconnect line will turn on the transistor slightly (causing a leakage path). Channel-stop implant raises Vth of parasitic transistor to a very large value.
- Create a stack of silicon oxide, silicon nitride, and positive PR



CMOS/Process steps

– Process step: Channel-stop implant (2)

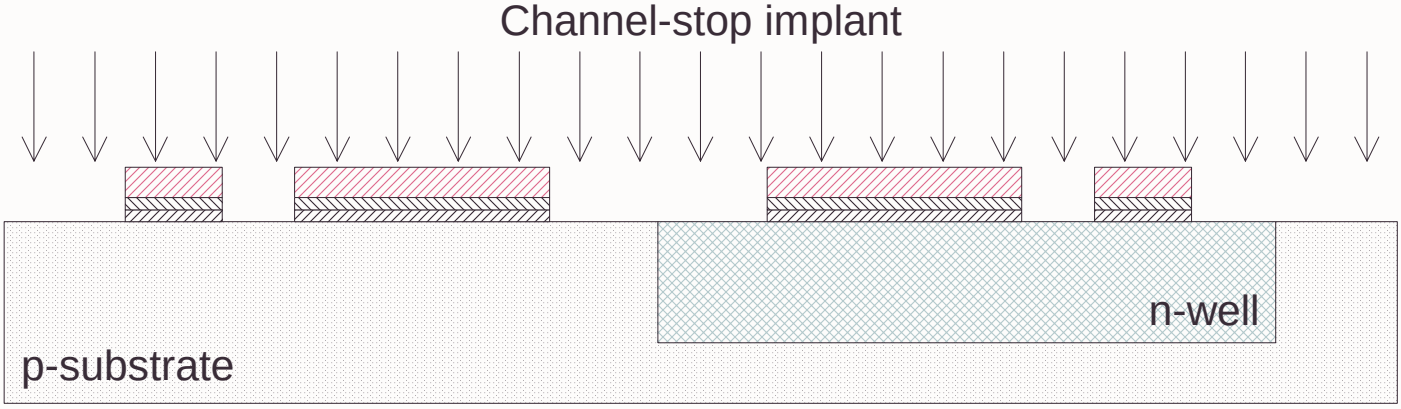
- Lithography sequence for channel-stop implant (based on positive PR)
- "Active" mask is used
  Active or diffusion areas include the source/drain regions and the p+ and n+ openings for the substrate and well ties



CMOS/Process steps

– Process step: Channel-stop implant (3)

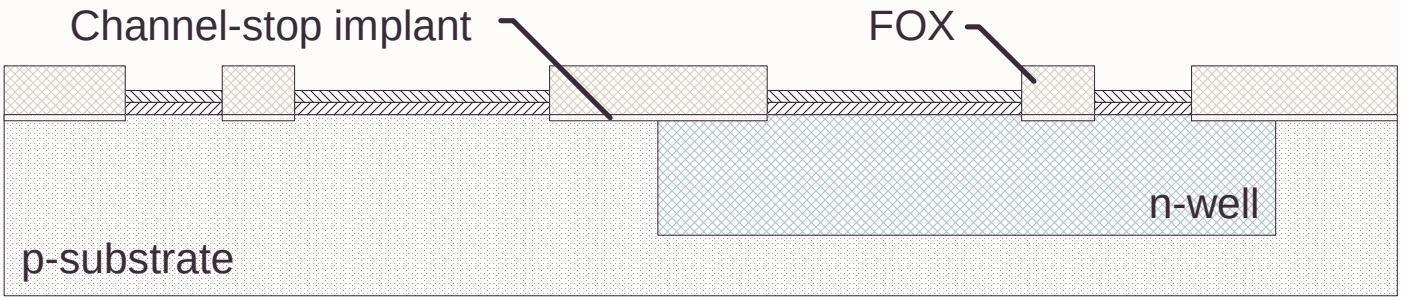
- Perform channel-stop ion implantation



CMOS/Process steps

– Process step: Channel-stop implant (4)

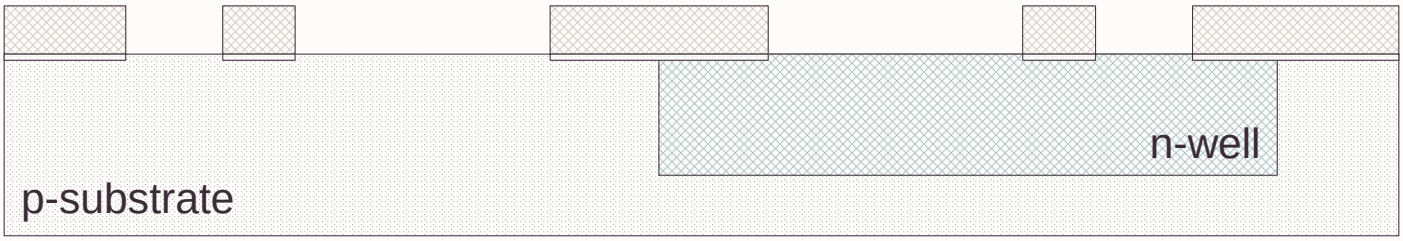
- Remove PR
- Thick oxide layer is grown in the exposed silicon areas producing the field oxide (FOX)
  FOX grows in areas where the silicon nitride layer is absent



CMOS/Process steps

– Process step: Channel-stop implant (5)

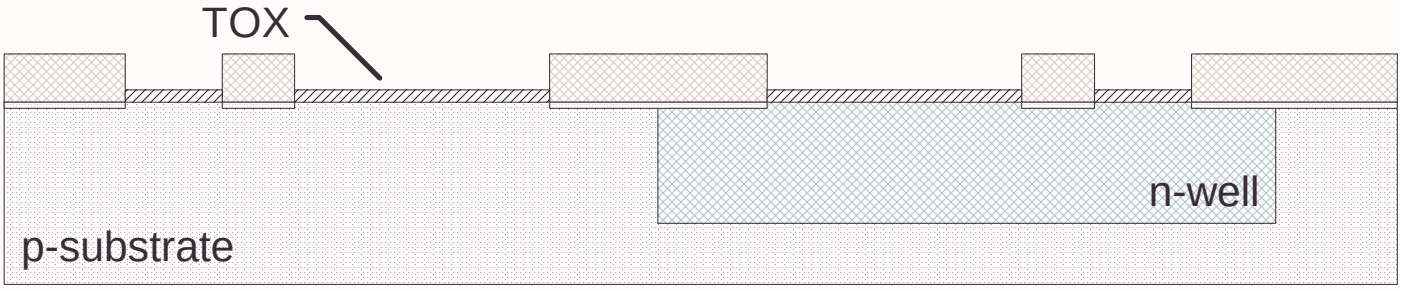
- Remove protective silicon nitride layer
- Remove protective thin oxide layer
- Result: Active areas are exposed



CMOS/Process steps

– Process step: Growth of gate oxide

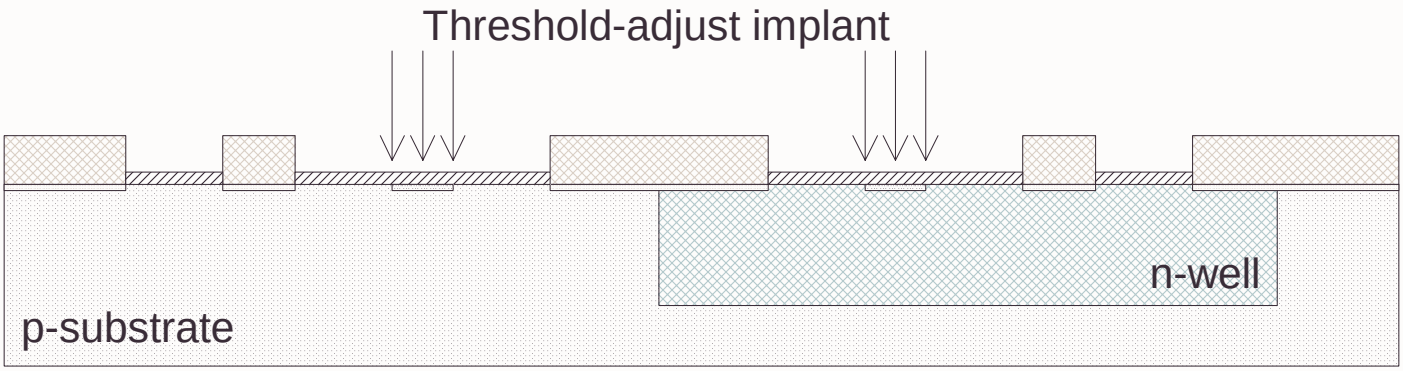
- Growth of gate oxide serving as gate dielectric (TOX)
  The growth of the gate oxide is a very critical step in the process. It's thickness t_{ox} determines a multitude of parameters of mosfets (current handling, transconductance, reliability). In order to achieve good matching of transistors extremely uniform thickness across the wafer is required. The oxide is therefore grown in a slow low-pressure CVD (chemical vapor deposition) process. Also, the cleanness of the silicon surface underneath the oxide affects the electrical behaviour of the mosfet.



CMOS/Process steps

– Process step: Threshold-adjust implant

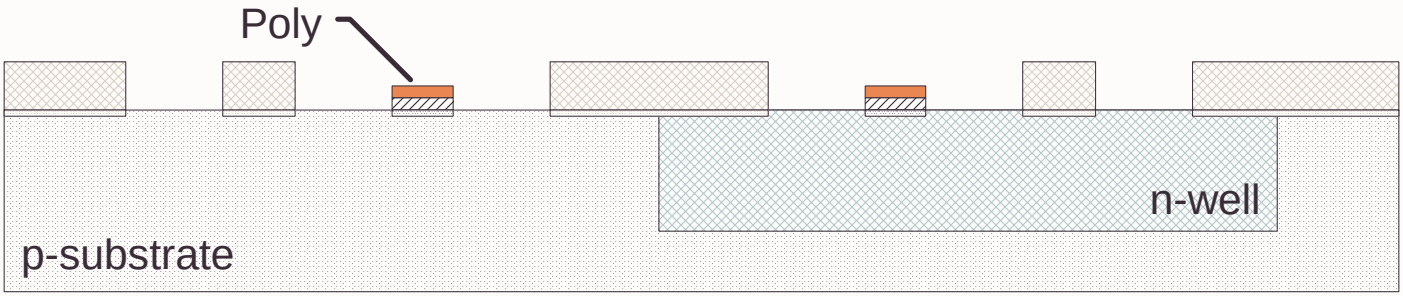
- Threshold-adjust implant after photolithographic process
  The "native" threshold voltage of transistors is typically far from the desired value (V_{THN}≈0V and V_{THP} ≈ -1V). A thin layer of dopants near the surface is implanted to adjust the native threshold voltage. Thresholds of both NMOS and PMOS transistors will become more positive.



CMOS/Process steps

– Process step: Create polysilicon (poly) layer

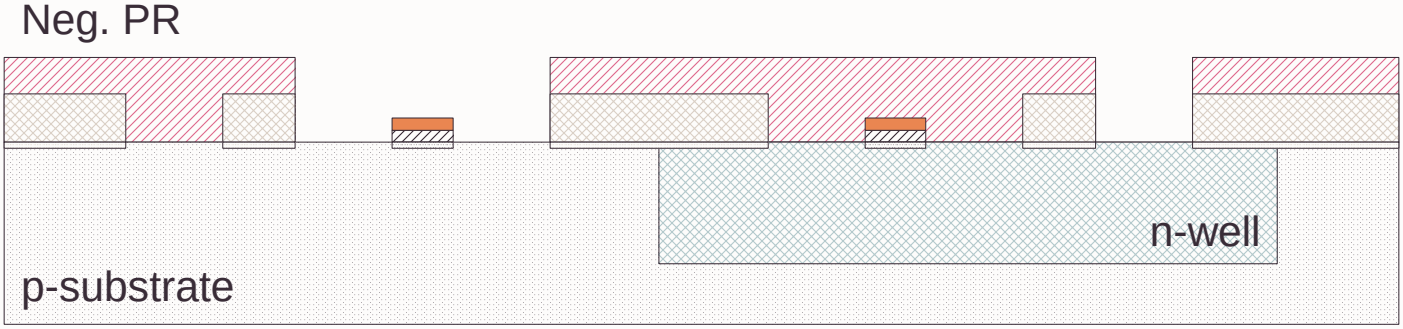
- Deposit a layer of polysilicon on top of the gate oxide
  Polysilicon is noncrystalline (or “amorphous”) silicon because this layer grows on top of silicon dioxide, i.e. cannot form a crystal. Since polysilicon only serves as a conductor its amorphous nature is unimportant.
- Carry out “poly mask” lithography



CMOS/Process steps

– Process step: n-type implant (1)

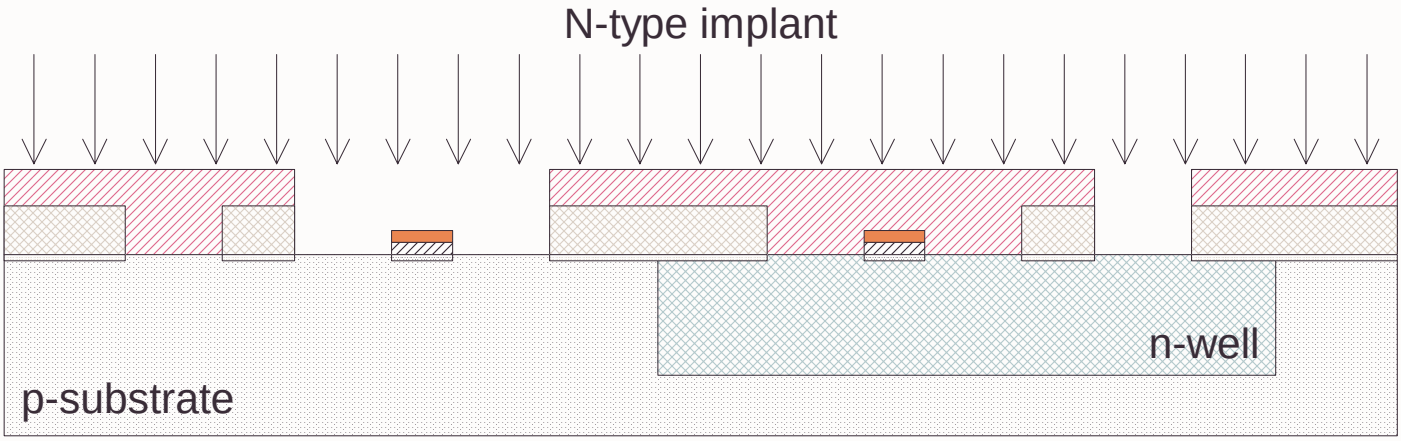
- Deposit negative photoresist
- Photolithography using “N source/drain mask”
  After the photolithography all areas to receive an n+ implant are exposed. These areas consist of source and drain junctions of NMOS transistors, and the n-well ties.



CMOS/Process steps

– Process step: n-type implant (2)

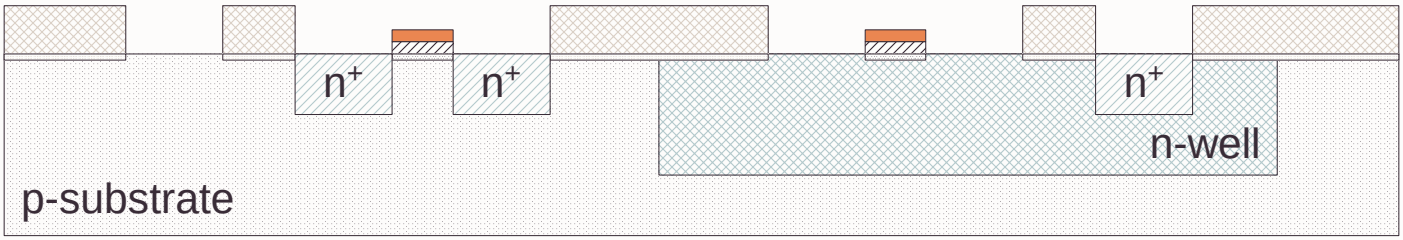
- Ion implantation
  Ion implantation forms the S/D regions of NMOS transistors and n-well ties. Note that the implant also dopes the polysilicon layer of the NMOS transistors, reducing its sheet resistance.



CMOS/Process steps

– Process step: n-type implant (3)

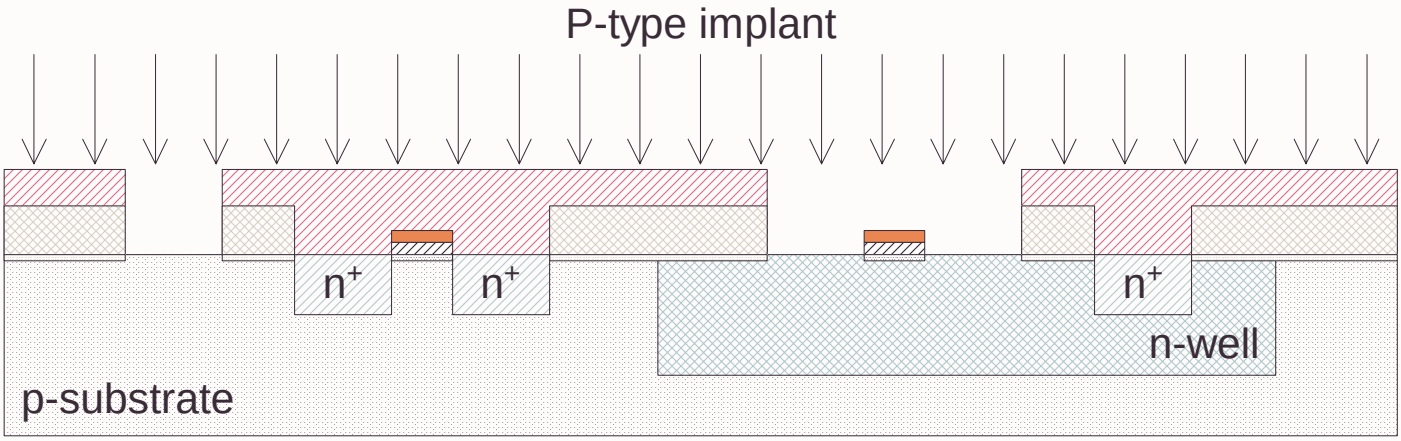
- Remove PR
- Self-aligned structure
  The sequence of creating the gates first prior to n-type implantation yields a self-aligned structure. The S/D regions are implanted at precisely the dges of the gate area. A misalignment in lithography simply makes one junction slightly narrower than the other.



CMOS/Process steps

– Process step: p-type implant (1)

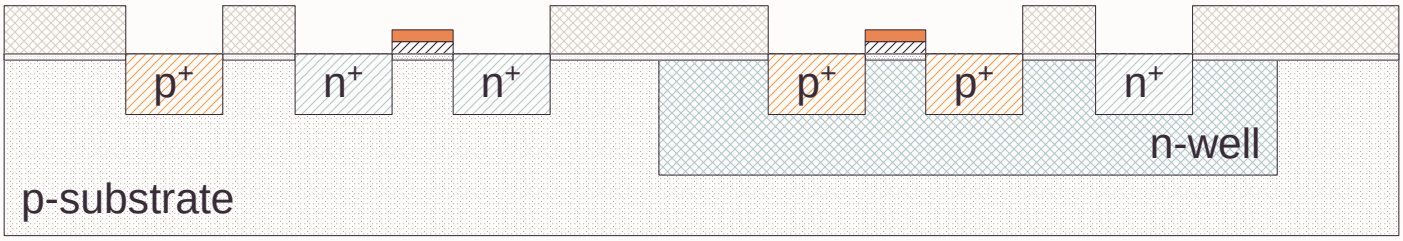
- Photolithography sequence using “P source/drain mask”
  After the photolithography all areas to receive an p+ implant are exposed. These areas consist of source and drain junctions of PMOS transistors, and the substrate ties.
- Ion implantation
  The implant also dopes the polysilicon layer of the PMOS transistors, reducing its sheet resistance



CMOS/Process steps

– Process step: p-type implant (2)

- Remove PR
- Basic transistor fabrication complete
- Remaining processing steps: “Back-end processing”

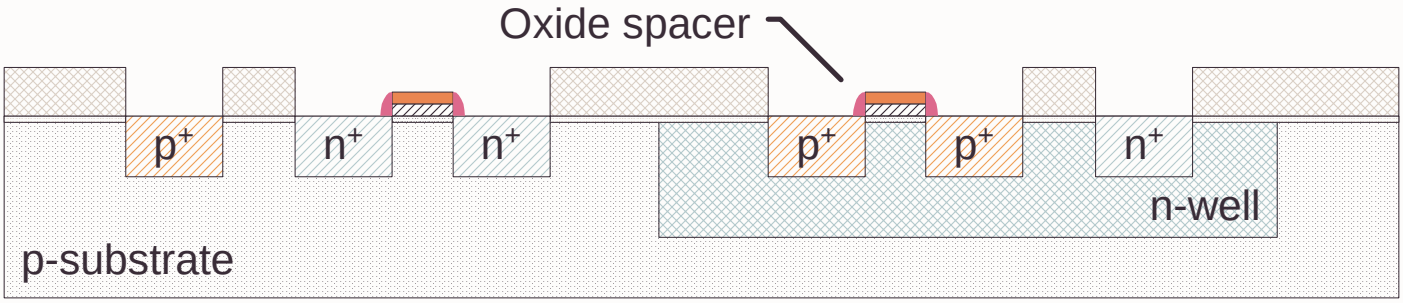


CMOS/Process steps

– Process step: Silicidation (1)

- Creation of oxide spacer

  Purpose of Silicidation: Reduction of sheet resistance of doped polysilicon and S/D regions by about an order of magnitude. During silicidation active areas (S/D regions, substrate and well ties) are covered with a thin layer of highly conductive material (titanium silicide or tungsten). The silicidation process begins with creating an oxide spacer at the edges of the polysilicon gate such that the deposition of the silicide will not short the gate to the S/D regions.

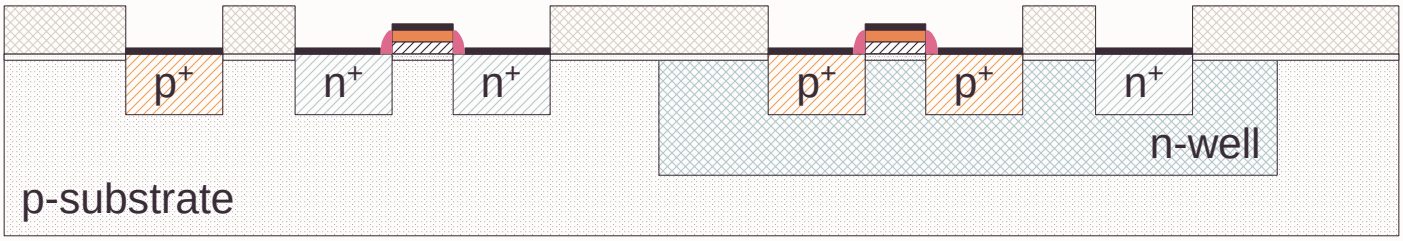


CMOS/Process steps

– Process step: Silicidation (2)

- Silicidation

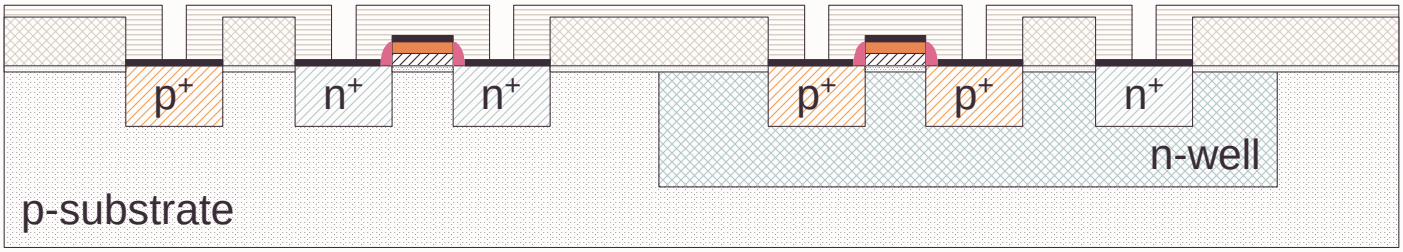
  Deposition of conductive material through CVD process



CMOS/Process steps

– Process step: Contact windows

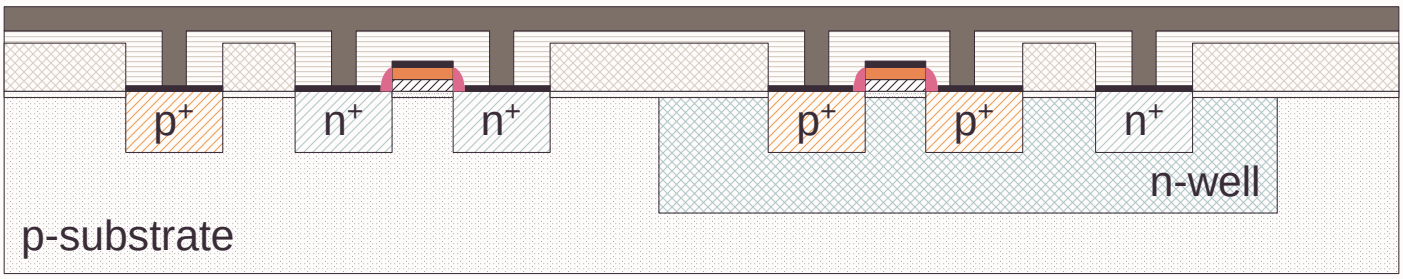
- Cover wafer with a thick layer of oxide
  Thickness: 300-500nm
- Lithography using the “contact mask”
- Plasma etching
  For increased reliability contacts to the gate polysilicon are not placed on top of the gate area



CMOS/Process steps

– Process step: Metal interconnect 1 (1)

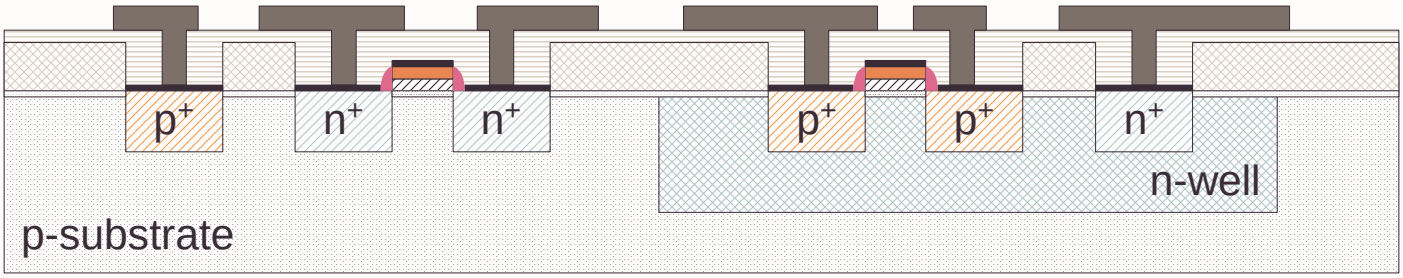
- Deposit layer of metal over the entire wafer
  Common metals: Aluminium or copper



CMOS/Process steps

– Process step: Metal interconnect 1 (2)

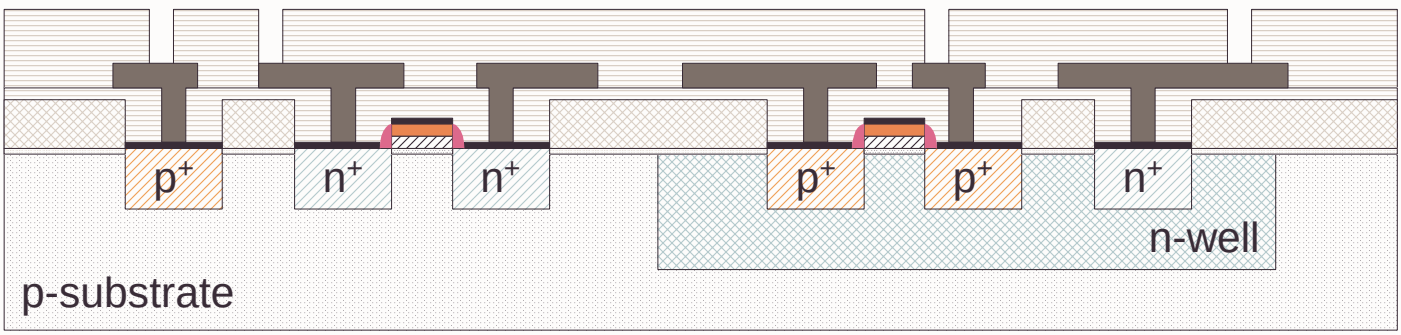
- Photolithography sequence using “Metal 1 mask”
- Metal selectively etched



CMOS/Process steps

– Process step: Via windows

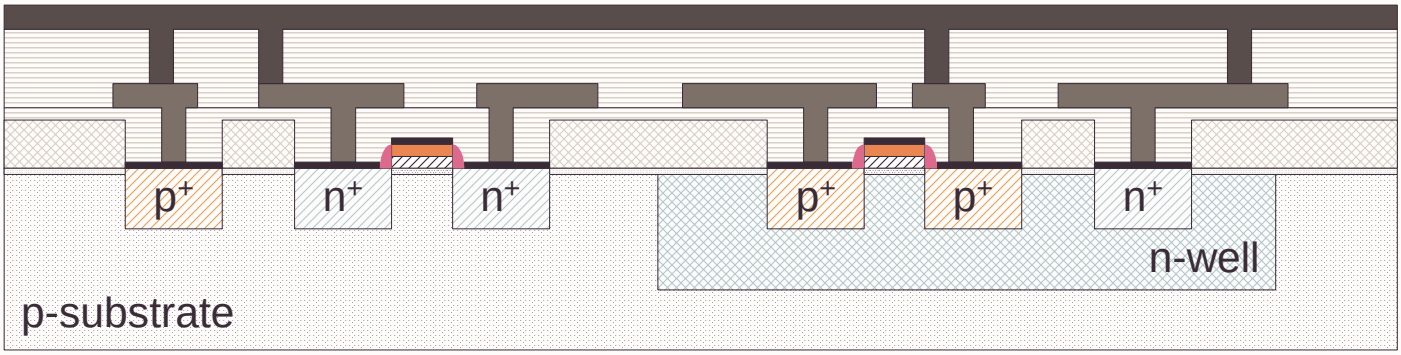
- Cover wafer with a layer of SiN_3
- Lithography using the “via mask”
- Plasma etching



CMOS/Process steps

– Process step: Metal interconnect 2 (1)

- Deposit layer of metal over the entire wafer



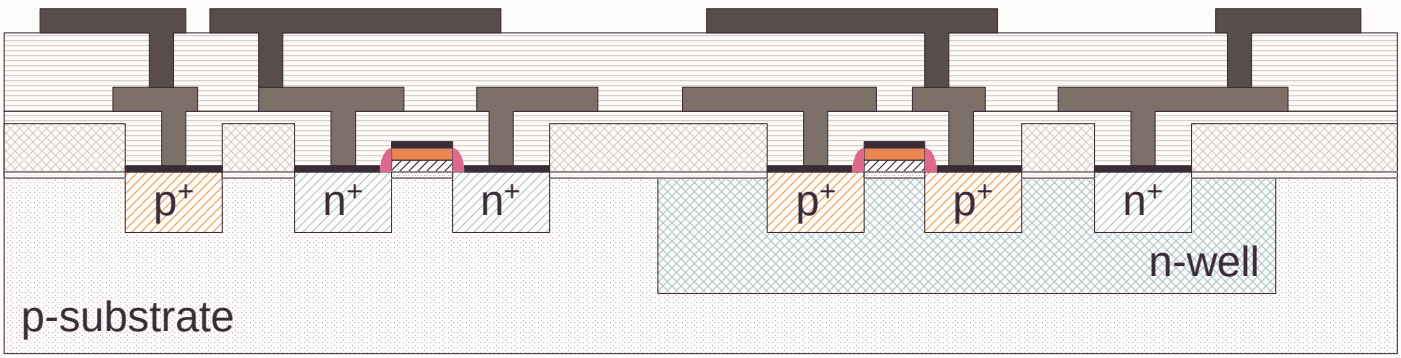
CMOS/Process steps

– Process step: Metal interconnect 2 (2)

- Photolithography sequence using “Metal 2 mask”
- Metal selectively etched

– Metal interconnect layers:

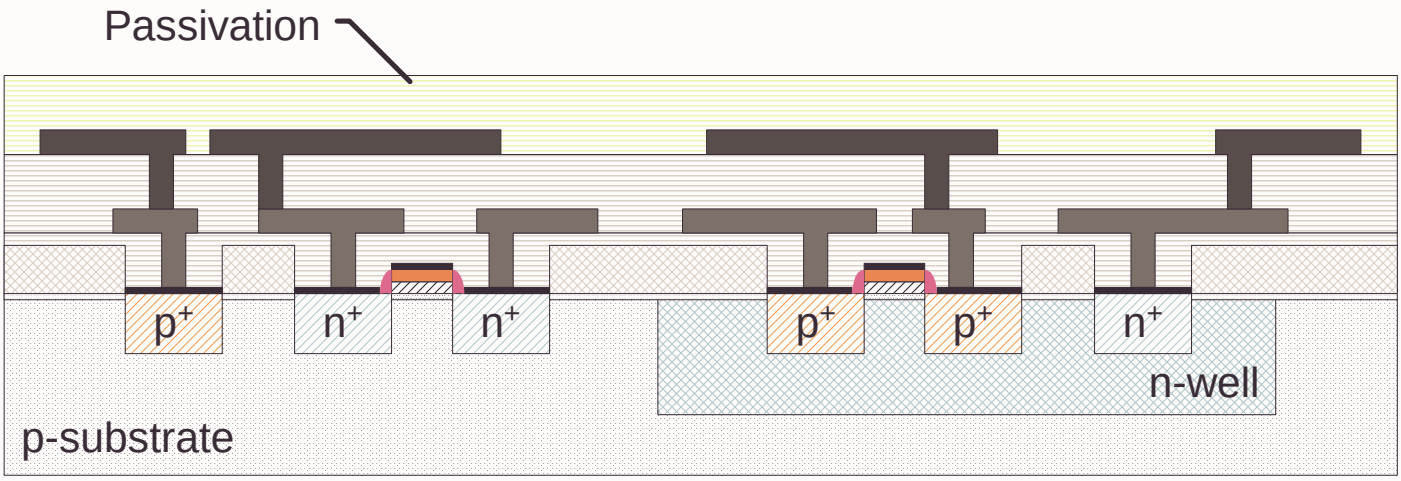
- Two masks required for each additional metal layer: “via *n* mask” and “metal *n* mask”
- Reliability: Dimensions of contacts/vias cannot be changed by layout designer (to avoid “contact spiking”). If a large contact area is required, small contacts/vias are used in parallel.



CMOS/Process steps

– Process step: Passivation

- Passivation
  Wafer is covered with a layer of “glass” or “passivation”, protecting the surface against damages caused by subsequent mechanical handling and dicing.



CMOS/Process steps

– Process step: Contact windows for bond pads

- Photolithography sequency

– Final processing steps:

- Testing, dicing, packaging, bonding, testing.