CMOS INVERTER

The Ideal Gate

\[ R_i = \infty \]
\[ R_o = 0 \]
DC Operation: Voltage Transfer Characteristic

Nominal Voltage Levels

Switching Threshold

CMOS Inverter VTC

V_{out}

V_{in}

NMOS off
PMOS lin

NMOS sat
PMOS lin

NMOS sat
PMOS sat

NMOS lin
PMOS sat

NMOS lin
PMOS off
Mapping between analog and digital signals

"1"  
\[ V_{OH}, V_{IH} \]  
Undefined Region

"0"  
\[ V_{IL}, V_{OL} \]

Definition of Noise Margins

\[ NM_H = V_{OH} - V_{IH} \] (High input)
\[ NM_L = V_{OL} - V_{IL} \] (Low input)
Fan-in and Fan-out

(a) Fan-out $N$

(b) Fan-in $M$

The CMOS Inverter: A First Glance
Delay Definitions

Vin

Vout

50%

50%

VDD

GND

1.2µm
=2λ

PMOS

NMOS

Polysilicon

Metal1

In

Out

Digital Integrated Circuits

Inverter

© Prentice Hall 1995

CMOS Inverters

Digital Integrated Circuits

Inverter

© Prentice Hall 1995
Switch Model of CMOS Transistor

Inverter

CMOS Inverter: Steady State Response

\[ V_{in} = V_{DD} \]
\[ V_{out} = V_{DD} \]
\[ V_{OL} = 0 \]
\[ V_{OH} = V_{DD} \]
\[ V_M = f(R_{on}, R_{onp}) \]
CMOS Inverter: Transient Response

\[ t_{\text{PHL}} = f(R_{\text{on}} \cdot C_L) = 0.69 \, R_{\text{on}} C_L \]

CMOS Inverter Propagation Delay

\[ t_{\text{PHL}} = \frac{C_L \, V_{\text{swing}} / 2}{I_{\text{av}}} \]

\[ \sim \frac{C_L}{k_n \, V_{\text{DD}}} \]
Dynamic Behavior of MOS Transistor

\[ \begin{align*}
G & \quad C_{GS} \\
S & \quad C_{SB} \\
\quad C_{GB} \\
D & \quad C_{GD} \\
B & \quad C_{DB}
\end{align*} \]

The Gate Capacitance

\[ C_{Gate} = \frac{W}{t_{ox}} \]

(a) Top view
(b) Cross-section
**Average Gate Capacitance**

Different distributions of gate capacitance for varying operating conditions

<table>
<thead>
<tr>
<th>Operation Region</th>
<th>$C_{gh}$</th>
<th>$C_{gs}$</th>
<th>$C_{gd}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cutoff</td>
<td>$C_{ox} W_{L_{eff}}$</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Triode</td>
<td>0</td>
<td>$C_{ox} W_{L_{eff}}/2$</td>
<td>$C_{ox} W_{L_{eff}}/2$</td>
</tr>
<tr>
<td>Saturation</td>
<td>0</td>
<td>$(2/3) C_{ox} W_{L_{eff}}$</td>
<td>0</td>
</tr>
</tbody>
</table>

Most important regions in digital design: saturation and cut-off

**Diffusion Capacitance**

Channel-stop implant

$$C_{diff} = C_{bottom} + C_{sw} = C_j \times \text{AREA} + C_{jsw} \times \text{PERIMETER}$$

$$C_{diff} = C_j L_S W + C_{jsw} (2L_S + 2W)$$
Junction Capacitance

\[ C_J = \frac{C_{j0}}{(1 - V_D / \phi_0)^m} \]

Linearizing the Junction Capacitance

Replace non-linear capacitance by large-signal equivalent linear capacitance which displaces equal charge over voltage swing of interest.

\[ C_{eq} = \frac{\Delta Q_j}{\Delta V_D} = \frac{Q_j(V_{\text{high}}) - Q_j(V_{\text{low}})}{V_{\text{high}} - V_{\text{low}}} = K_{eq} C_{j0} \]

\[ K_{eq} = \frac{-\phi_0^m}{(V_{\text{high}} - V_{\text{low}})(1 - m)} \left[ (\phi_0 - V_{\text{high}})^{1-m} - (\phi_0 - V_{\text{low}})^{1-m} \right] \]
The Miller Effect

“A capacitor experiencing identical but opposite voltage swings at both its terminals can be replaced by a capacitor to ground, whose value is two times the original value.”

Computing the Capacitances

Simplified Model

Fanout
## Computing the Capacitances

<table>
<thead>
<tr>
<th>Capacitor</th>
<th>Expression</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_{gd1}$</td>
<td>$2 \text{CGD0 } W_n$</td>
</tr>
<tr>
<td>$C_{gd2}$</td>
<td>$2 \text{CGD0 } W_p$</td>
</tr>
<tr>
<td>$C_{db1}$</td>
<td>$K_{eqn} (AD_n CJ + PD_n CJSW)$</td>
</tr>
<tr>
<td>$C_{db2}$</td>
<td>$K_{eqp} (AD_p CJ + PD_p CJSW)$</td>
</tr>
<tr>
<td>$C_{g3}$</td>
<td>$C_{ox} W_n L_n$</td>
</tr>
<tr>
<td>$C_{g4}$</td>
<td>$C_{ox} W_p L_p$</td>
</tr>
<tr>
<td>$C_w$</td>
<td>From Extraction</td>
</tr>
<tr>
<td>$C_L$</td>
<td>$\Sigma$</td>
</tr>
</tbody>
</table>

## Capacitances: Typical values

**Table 3.5** Capacitance parameters of NMOS and PMOS transistors in 0.25 μm CMOS process.

<table>
<thead>
<tr>
<th></th>
<th>$C_{ox}$ (fF/μm²)</th>
<th>$C_o$  (fF/μm)</th>
<th>$C_j$  (fF/μm²)</th>
<th>$m_j$</th>
<th>$\phi_b$ (V)</th>
<th>$C_{jsw}$ (fF/μm)</th>
<th>$m_{jsw}$</th>
<th>$\phi_{b_{sw}}$ (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>NMOS</td>
<td>6</td>
<td>0.31</td>
<td>2</td>
<td>0.5</td>
<td>0.9</td>
<td>0.28</td>
<td>0.44</td>
<td>0.9</td>
</tr>
<tr>
<td>PMOS</td>
<td>6</td>
<td>0.27</td>
<td>1.9</td>
<td>0.48</td>
<td>0.9</td>
<td>0.22</td>
<td>0.32</td>
<td>0.9</td>
</tr>
</tbody>
</table>