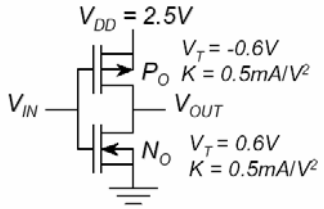
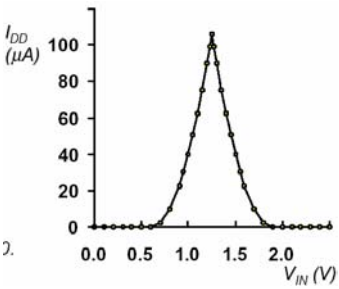
DC Current in CMOS

- For $V_{IN} < V_{TN}$, N_O is cut off and $I_{DD} = 0$.
- For $V_{TN} < V_{IN} < V_{DD}/2$, N_O is saturated.
- For $V_{DD}/2 < V_{IN} < V_{DD}+V_{TP}$, P_O is saturated.
- For $V_{IN} > V_{DD} + V_{TP}$, P_O is cut off and $I_{DD} = 0$.
- • For $V_{DD}/2 < V_{IN} < V_{DD}+V_{TP}$, P_O is saturated.
- • For $V_{IN} > V_{DD} + V_{TP}$, P_O is cut off and $I_{DD} = 0$.
- Even though CMOS exhibits negligible DC dissipation in either logic state, appreciable power is dissipated during switching.

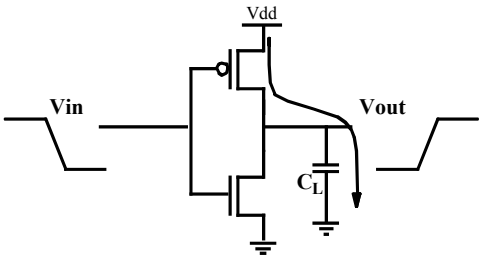


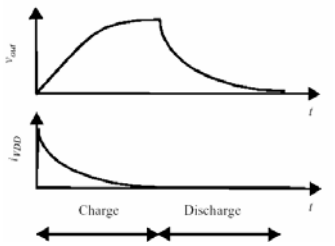


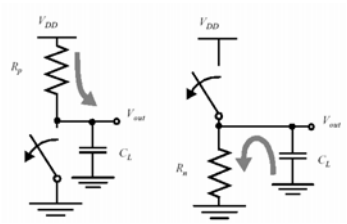
Power dissipation in CMOS

- **Dynamic Power Consumption**
  - **Charging and Discharging Capacitors**
- **Short Circuit Currents**
  - **Short Circuit Path between Supply Rails during Switching**
- **Leakage**
  - **Leaking diodes and transistors**

Dynamic Power Dissipation







Capacitor Energy:

$E_C = 1/2\ C\ V_{dd}^2$

Dynamic Power Dissipation

For each transition (clock cycle):

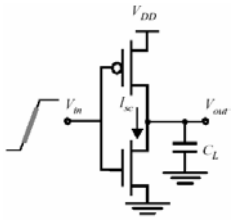
$$\textbf{Energy/transition} = C_L * V_{dd}^2$$

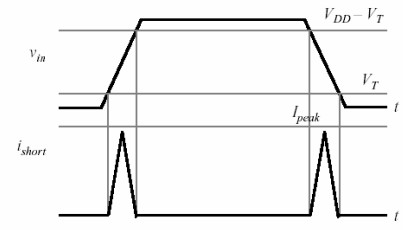
$$\textbf{Power} = \textbf{Energy/transition} * f = C_L * V_{dd}^2 * f$$

- **Not a function of transistor sizes**
- **Need to reduce C_L, V_{dd} and f to reduce power.**

Dissipation Due to Direct-Path Currents

- during switching the NMOS and the PMOS transistors are conducting simultaneously.
- This puts the power supply in "short-circuit" during the transitions of the input signal
- "short-circuit" current is limited by transistors current capacity ⇒ depends on transistor size



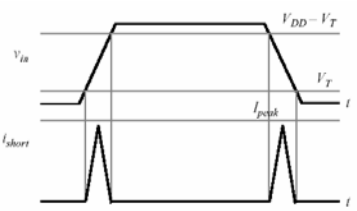


Dissipation Due to Direct-Path Currents

t_{sc}: shot circuit duration

$$t_{sc} = \frac{V_{DD}-2V_T}{V_{DD}} t_s \approx \frac{V_{DD}-2V_T}{V_{DD}} \times \frac{t_{r(f)}}{0.8}$$

$t_{r(f)}$: rise (fall) time of input signal (10%-90%)



$$E_{dp} = V_{DD}\frac{I_{peak}t_{sc}}{2} + V_{DD}\frac{I_{peak}t_{sc}}{2} = t_{sc}V_{DD}I_{peak}$$

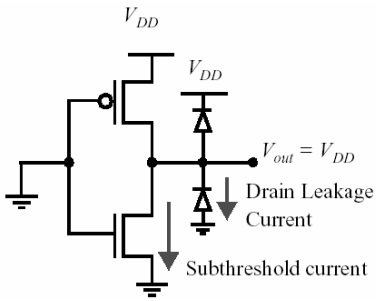
$$\boxed{P_{dp} = t_{sc}V_{DD}I_{peak}f}$$

I_{peak}: peak current of transistors ($Vo=V_{DD}/2$)

f: switching frequency

Dissipation Due to Leakage

- reverse-biased diode junctions and transistors leakage
- 10-100 pA/μm² at room temperature.
- Increases exponentially with temperature



$$P_{stat} = I_{stat} V_{DD}$$

I_{stat}: leakage currents

Total Power Dissipation

$$P_{tot} = P_{dyn} + P_{dp} + P_{stat}$$

$$P_{tot} = (C_L V_{DD}^2 + V_{DD} I_{peak} t_s) f_0 + V_{DD} I_{leak}$$

•*Low frequency operation:* P_{stat} *dominates*

•*High frequency operation:* P_{dyn}+P_{dp} *dominates*

CMOS Electrical Characteristics

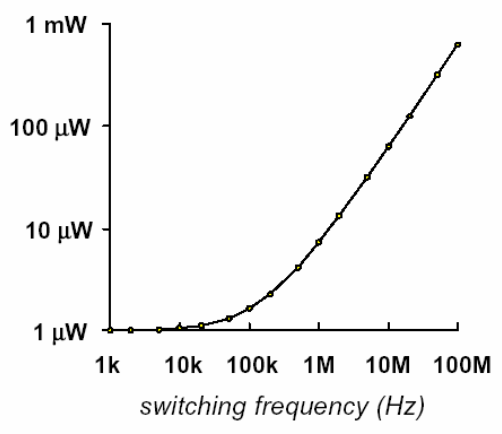
- Power-delay product
- Latch-up
- Hot carriers
- Electromigration
- Sheet resistance
- Parasitic capacitances

Power-delay product

- *Figure of merit to determine quality of a digital gate*
- *Power-delay product PDP: measures the energy of the gate [W.s=J]*

$$PDP = P_{av} t_p$$

- *PDP stands for the average energy consumed per switching event*



Power-delay product

- *Assuming that the gate is switched at its maximum possible rate f_{max}*

$$f_{max} = 1/(2t_p), \qquad t_p=(t_{pHL}+t_{pLH})/2$$

$$PDP = \frac{P_{av}}{2f_{\max}}$$

- *In high frequencies, power dissipation dominated by capacitive load C_L*

$$t_P \approx \frac{2C_L}{KV_{DD}}$$

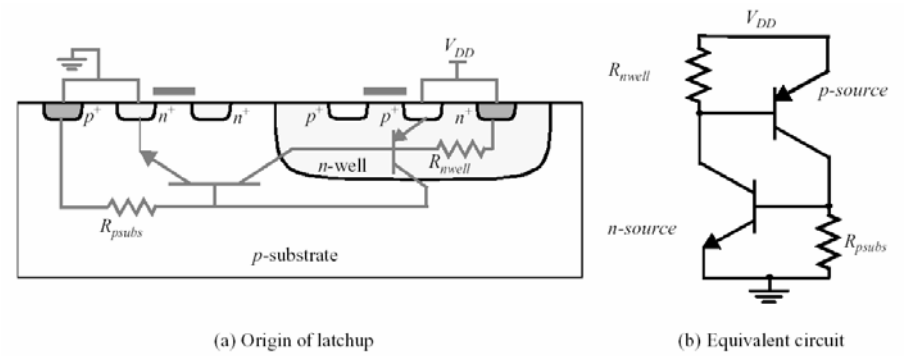
- *ignoring contributions of static and direct-path currents:*

$$PDP \approx \frac{2V_{DD}C_L^2 f}{K}$$

- *The design goal is to minimize PDP, in order to get low power in high frequencies*
- *Thus it is important to decrease V_{DD} but it is extremely important to decrease the load capacitance C_L*

Latch-up

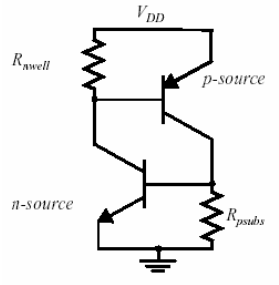
- *MOS technology contains intrinsic bipolar transistors*
- *in CMOS processes, combination of wells and substrates results in parasitic n-p-n-p structures.*



(a) Origin of latchup (b) Equivalent circuit

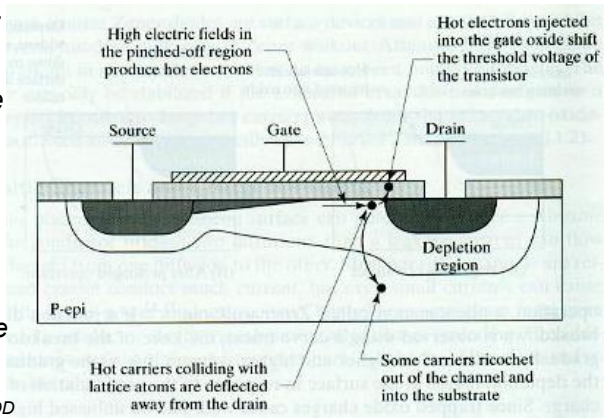
Latch-up

- *Triggering these SCR-like devices ⇒ short circuit between V_{DD} and V_{SS}*
- *Consequence: destruction of the chip, or at best system failure (can solved by power-down)*
- *To avoid latch-up:*
  - ✓*Keep low temperatures and low V_{DD} (temperature increases bipolar gain and leak currents)*
  - ✓*Decrease R_{nwell} and R_{psubs} ⇒ well and substrate contacts close to the source of NMOS/PMOS*



Hot carriers

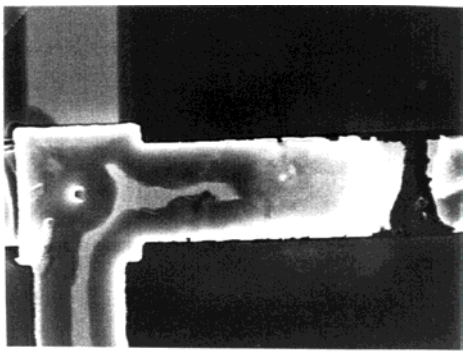
- *Small dimension MOSFET suffers from hot-carrier effect*
- *High velocity electrons leave the silicon and tunnel into the gate oxide*
- *Electrons trapped in oxide change threshold voltage V_T:*
  - *NMOS: V_{TN} ⇑*
  - *PMOS: $|V_{TP}|$ ⇓*
- *Can cause permanent dammage to the device*
- *Sensible to Temperature and V_{DD}*



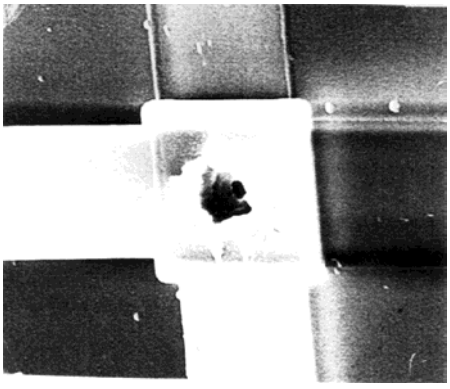
Electromigration

- Metal wire can tolerate only a certain amount of current density.
- Direct current for a long time causes ion movement breaking the wire over time.
- Contacts are more vulnerable to electromigration as the current tends to run through the perimeter.
- Possible solutions:
  - » Make wire cross section wider⇒increase width/depth (reduce current density)
  - » Use of copper instead of Al (heavier ions)

Electromigration example



A wire broken off due to electromigration



A contact (via) broken up due to electromigration

These figures are derived from *Digital integrated circuit – a design perspective*, J. Rabaey Prentice Hall

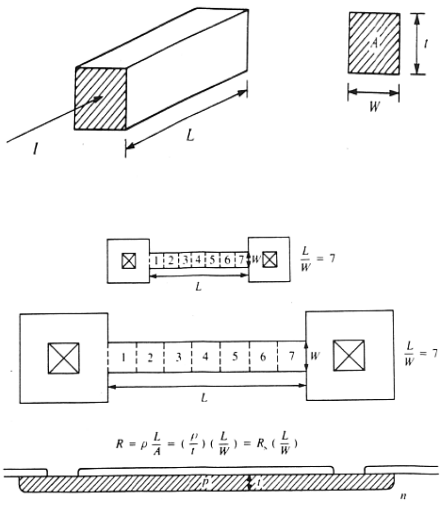
Current limits

- Electromigration
- Power density: heating due to Joule effect
- Respect max current densities to each layer (specified by the technology design rules)

Sheet resistance R_S

- Resistivity of materials are given in ohms/square (Ω/□)
- Easier way to compute resistance due to uniform depth of conducting/semiconducting layers
- To calculate the resistance of a line:
  - » Divide the line in squares
  - » Multiply the number of squares by the given value of R_S in Ω/□

$$R = \rho \frac{L}{A} = \left(\frac{\rho}{t}\right)\left(\frac{L}{W}\right) = R_s\left(\frac{L}{W}\right)$$

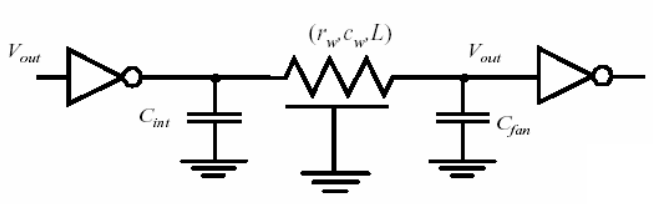


Parasitic capacitances

- Conducting lines over substrate or crossing forms parasitic capacitances
- Can be very important for long lines
- Increase power dissipated and PDP

- To calculate the capacitance of two crossing lines:
  - » Calculate the total crossing area
  - » Multiply by the given value of C per area in μF/μm^2

Delay in the Presence of (Long) Interconnect Wires



$t_{pHL} = f(R_{on}.C_L)$
$= 0.69\ R_{on}C_L$

ln(0.5)

$$t_p = 0.69R_{dr}C_{int} + (0.69R_{dr} + 0.38R_w)C_w + 0.69(R_{dr} + R_w)C_{fan}$$
$$= 0.69R_{dr}(C_{int} + C_{fan}) + 0.69(R_{dr}c_w + r_w C_{fan})L + 0.38r_w c_w L^2$$