CMOS Electrical Characteristics

- Power-delay product
- Latch-up
- Hot carriers
- Electromigration
- Sheet resistance
- Parasitic capacitances

Power-delay product

- Figure of merit to determine quality of a digital gate
- Power-delay product (PDP) measures the energy of the gate [W.s/J]
  \[ PDP = P_{av} t_p \]
- PDP stands for the average energy consumed per switching event

Power-delay product

- Assuming that the gate is switched at its maximum possible rate \( f_{max} \)
  \[ f_{max} = f(t_{phLL} + t_{phHL}) / 2 \]
- In high frequencies, power dissipation dominated by capacitive load \( C_L \)
- Ignoring contributions of static and direct-path currents:
  \[ PDP = \frac{P_{av}}{2f_{max}} \]
- The design goal is to minimize PDP, in order to get low power in high frequencies
- Thus it is important to decrease \( V_{dd} \) but it is extremely important to decrease the load capacitance \( C_L \)

Latch-up

- MOS technology contains intrinsic bipolar transistors
- In CMOS processes, combination of wells and substrates results in parasitic n-p-n-p structures.
Latch-up

- Triggering these SCR-like devices ⇒ short circuit between VDD and VSS
- Consequence: destruction of the chip, or at best system failure (can solved by power-down)
- To avoid latch-up:
  - Keep low temperatures and low VDD (temperature increases bipolar gain and leak currents)
  - Decrease Rnwell and Rpsubs ⇒ well and substrate contacts close to the source of NMOS/PMOS

Hot carriers

- Small dimension MOSFET suffers from hot-carrier effect
- High velocity electrons leave the silicon and tunnel into the gate oxide
- Electrons trapped in oxide change threshold voltage $V_T$
  - NMOS: $V_{TN}$↑
  - PMOS: $|V_{TP}|$↓
- Can cause permanent damage to the device
- Sensible to Temperature and VDD

Electromigration

- Metal wire can tolerate only a certain amount of current density.
- Direct current for a long time causes ion movement breaking the wire over time.
- Contacts are more vulnerable to electromigration as the current tends to run through the perimeter.
- Possible solutions:
  - Make wire cross section wider ⇒ increase width/depth (reduce current density)
  - Use of copper instead of Al (heavier ions)
Current limits

- Electromigration
- Power density: heating due to Joule effect
- Respect max current densities to each layer (specified by the technology design rules)

Sheet resistance $R_S$

- Resistivity of materials are given in ohms/square ($\Omega/\square$)
- Easier way to compute resistance due to uniform depth of conducting/semiconducting layers
- To calculate the resistance of a line:
  - Divide the line in squares
  - Multiply the number of squares by the given value of $R_S$ in $\Omega/\square$

\[
R = \frac{L}{w} \cdot \frac{L}{w} \cdot R_S
\]

Parasitic capacitances

- Conducting lines over substrate or crossing forms parasitic capacitances
- Can be very important for long lines
- Increase power dissipated and PDP
- To calculate the capacitance of two crossing lines:
  - Calculate the total crossing area
  - Multiply by the given value of $C$ per area in $\mu F/\mu m^2$

Delay in the Presence of (Long) Interconnect Wires

\[
\tau_p = 0.69 R_{on} C_{int} + (0.69 R_{dr} + 0.38 R_{on}) C_{int} + 0.69 (R_{df} + R_{on}) C_{fan}
\]

\[
= 0.69 R_{on} (C_{int} + C_{fan}) + 0.69 (R_{df} C_{int} + R_{on} C_{fan}) L + 0.38 r_w C_{int} L^2
\]