CMOS Electrical Characteristics

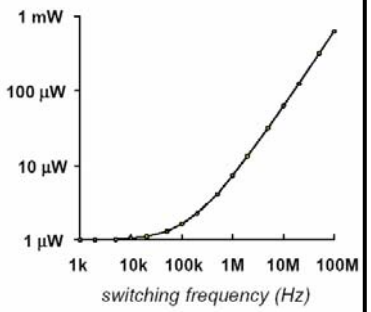
- Power-delay product
- Latch-up
- Hot carriers
- Electromigration
- Sheet resistance
- Parasitic capacitances

Power-delay product

- *Figure of merit to determine quality of a digital gate*
- *Power-delay product PDP: measures the energy of the gate [W.s=J]*

$$PDP = P_{av} t_p$$

- *PDP stands for the average energy consumed per switching event*



Power-delay product

- *Assuming that the gate is switched at its maximum possible rate f_{max}*

$$f_{max} = 1/(2t_p) \qquad t_p=(t_{pHL}+t_{pLH})/2$$

- *In high frequencies, power dissipation dominated by capacitive load C_L*
- *ignoring contributions of static and direct-path currents:*
- *The design goal is to minimize PDP, in order to get low power in high frequencies*
- *Thus it is important to decrease V_{DD} but it is extremely important to decrease the load capacitance C_L*

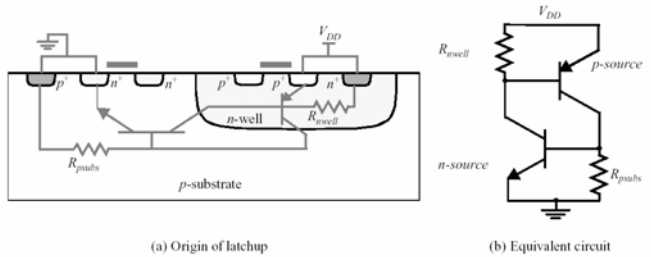
$$PDP = \frac{P_{av}}{2f_{max}}$$

$$t_P \approx \frac{2C_L}{KV_{DD}}$$

$$PDP \approx \frac{2V_{DD}C_L^2 f}{K}$$

Latch-up

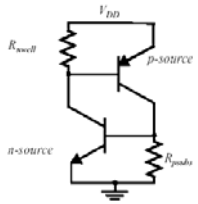
- *MOS technology contains intrinsic bipolar transistors*
- *in CMOS processes, combination of wells and substrates results in parasitic n-p-n-p structures.*



(a) Origin of latchup (b) Equivalent circuit

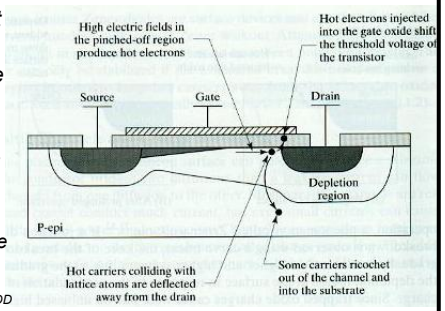
Latch-up

- *Triggering these SCR-like devices ⇒ short circuit between V_{DD} and V_{SS}*
- *Consequence: destruction of the chip, or at best system failure (can solved by power-down)*
- *To avoid latch-up:*
  - ✓*Keep low temperatures and low V_{DD} (temperature increases bipolar gain and leak currents)*
  - ✓*Decrease R_{nwell} and R_{psubs} ⟹ well and substrate contacts close to the source of NMOS/PMOS*



Hot carriers

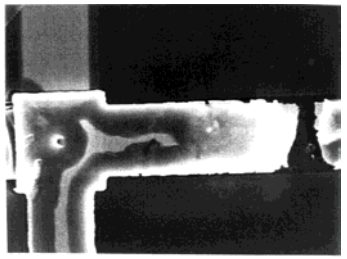
- *Small dimension MOSFET suffers from hot-carrier effect*
- *High velocity electrons leave the silicon and tunnel into the gate oxide*
- *Electrons trapped in oxide change threshold voltage V_T:*
  - *NMOS: V_{TN} ⇑*
  - *PMOS: $|V_{TP}|$ ⇓*
- *Can cause permanent dammage to the device*
- *Sensible to Temperature and V_{DD}*



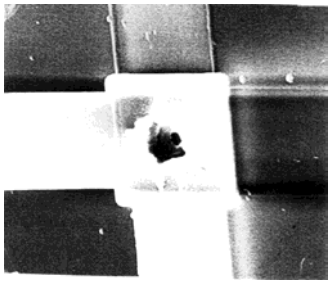
Electromigration

- Metal wire can tolerate only a certain amount of current density.
- Direct current for a long time causes ion movement breaking the wire over time.
- Contacts are more vulnerable to electromigration as the current tends to run through the perimeter.
- Possible solutions:
  - » Make wire cross section wider⇒increase width/depth (reduce current density)
  - » Use of copper instead of Al (heavier ions)

Electromigration example



A wire broken off due to electromigration



A contact (via) broken up due to electromigration

These figures are derived from *Digital integrated circuit – a design perspective*, J. Rabaey Prentice Hall

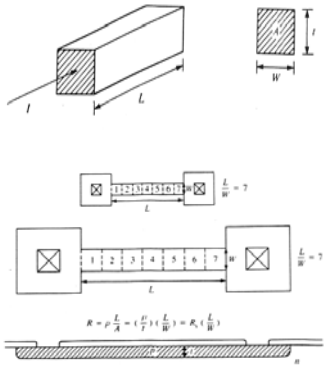
Current limits

- Electromigration
- Power density: heating due to Joule effect
- Respect max current densities to each layer (specified by the technology design rules)

Sheet resistance R_S

- Resistivity of materials are given in ohms/square (Ω/□)
- Easier way to compute resistance due to uniform depth of conducting/semiconducting layers
- To calculate the resistance of a line:
  - » Divide the line in squares
  - » Multiply the number of squares by the given value of R_S in Ω/□

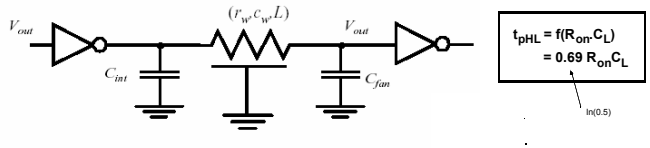
$$R = \rho \frac{L}{A} = \left(\frac{\rho}{t}\right)\left(\frac{L}{W}\right) = R_{\square}\left(\frac{L}{W}\right)$$



Parasitic capacitances

- Conducting lines over substrate or crossing forms parasitic capacitances
- Can be very important for long lines
- Increase power dissipated and PDP
- To calculate the capacitance of two crossing lines:
  - » Calculate the total crossing area
  - » Multiply by the given value of C per area in μF/μm²

Delay in the Presence of (Long) Interconnect Wires



$$t_p = 0.69R_{dr}C_{int} + (0.69R_{dr} + 0.38R_w)C_w + 0.69(R_{dr} + R_w)C_{fan}$$
$$= 0.69R_{dr}(C_{int} + C_{fan}) + 0.69(R_{dr}c_w + r_w C_{fan})L + 0.38r_w c_w L^2$$