Integridade de Sinais Elétricos

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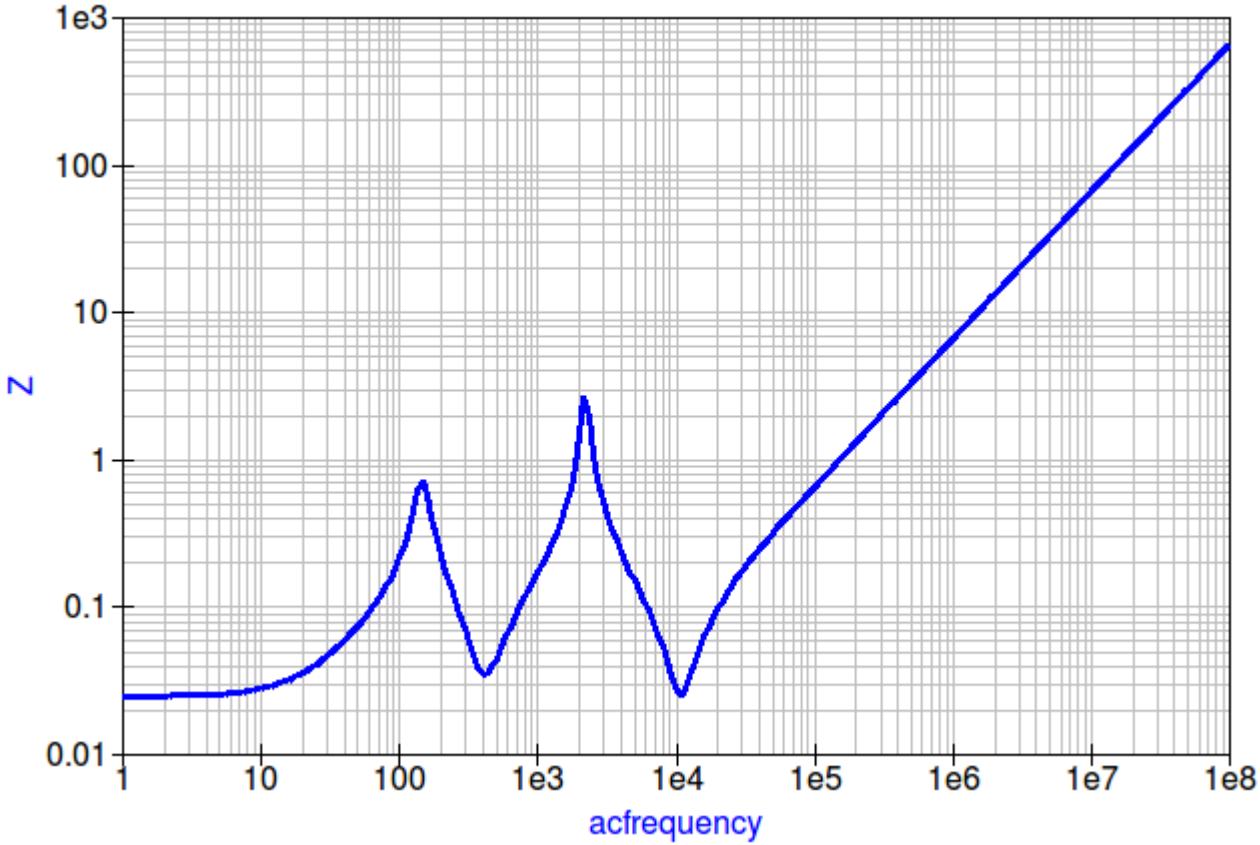
Problemas associados à alimentação de circuitos

- Fontes de alimentação (tensão) ideais possuem impedância nula em qualquer frequência
- Fontes de alimentação reais possuem impedância variável com a frequência
- Impedância da fonte é dominada por:
  - Baixas frequências (0 – 100 Hz): circuito de realimentação
  - Médias frequências (100 – 10 kHz): capacitores de filtro
  - Altas frequências (> 10 kHz): Indutância das conexões

Problemas associados à alimentação de circuitos

Impedância típica de fonte de alimentação regulada

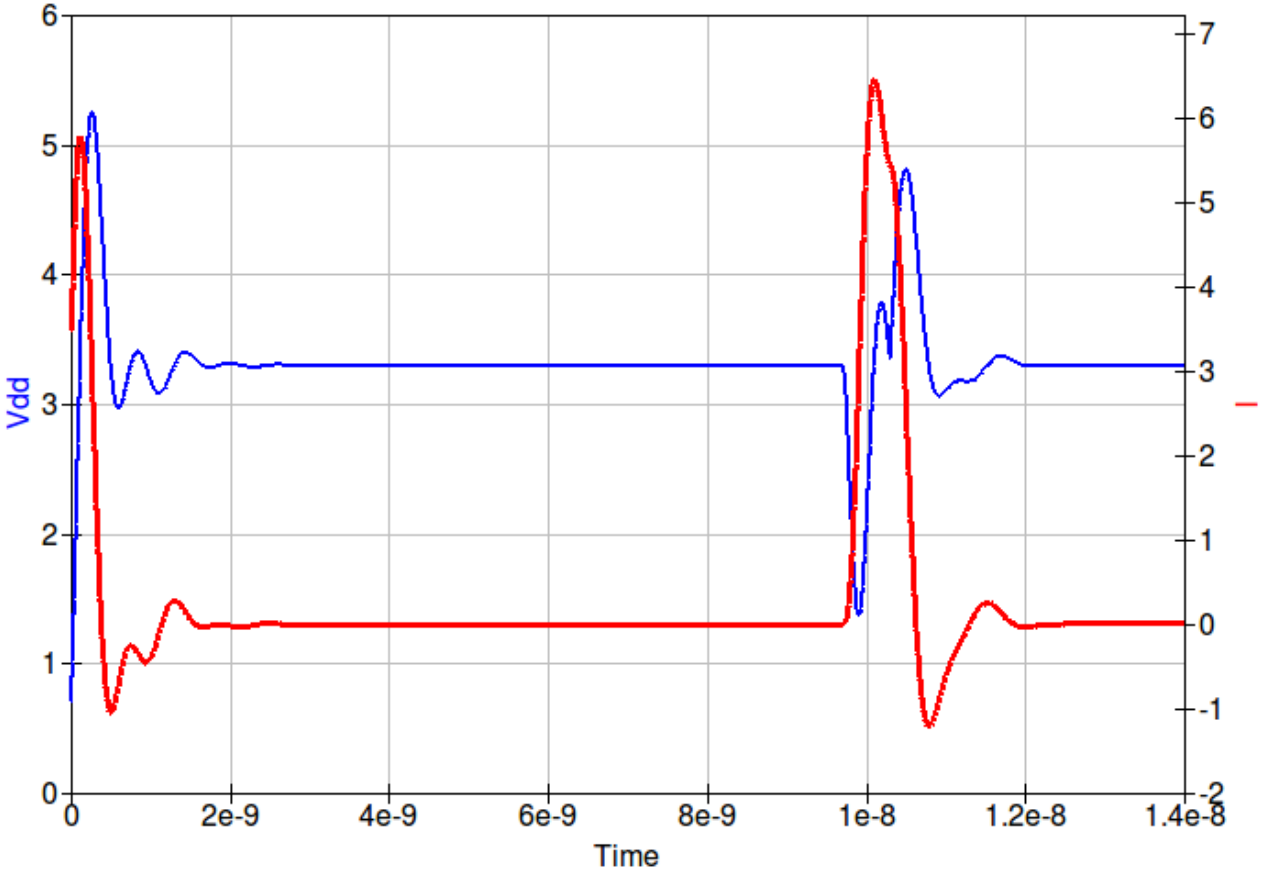


Problemas associados à alimentação de circuitos

- Circuitos de alta frequência geram transientes de corrente na sua alimentação
- Em particular os circuitos digitais CMOS geram transientes de corrente nas transições de nível lógico
- Um microprocessador atual chega a gerar transientes de corrente de centenas de Ampères em alguns ns
- Estes transientes de corrente geram variações rápidas na tensão de alimentação (ruídos)
- Ruídos na alimentação são grandes fontes de erro em circuitos digitais e de altas frequências e devem ser minimizados

Problemas associados à alimentação de circuitos

Tensão e corrente na alimentação de um circuito digital CMOS



Problemas associados à alimentação de circuitos

- Capacitores de filtro da alimentação são essenciais em circuitos de alta frequência
- Devem ser colocados o mais próximo possível dos circuitos para minimizar o efeito das indutâncias de conexão
- Deve-se levar em conta as não idealidades dos capacitores (indutância e resistência série)
- De modo geral são necessários vários capacitores em paralelo para atingir os objetivos de filtragem adequada
- O projeto destes capacitores leva em conta a impedância máxima permitida em determinada faixa de frequência ou o ruído máximo

We will begin in minutes

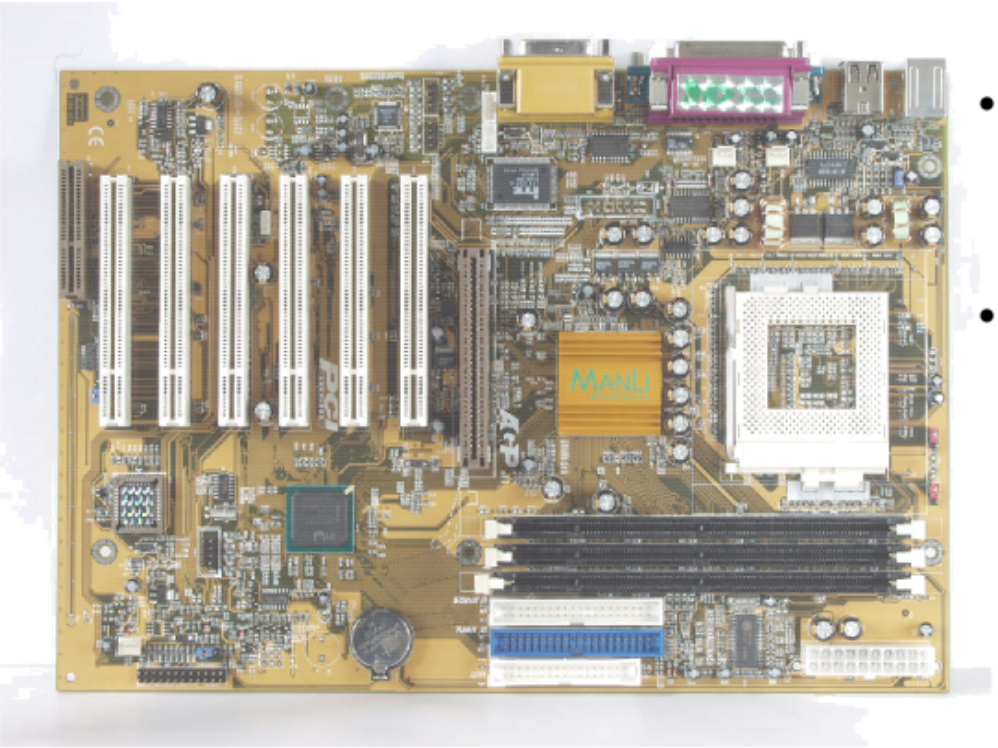
No Myths Allowed Webinar Series
NMA-840
Dec 9, 2009

Selecting Capacitors for the PDN

Eric Bogatin,
Signal Integrity Evangelist, Bogatin Enterprises
And
Larry Smith,
Signal Integrity Architect, Altera Corporation

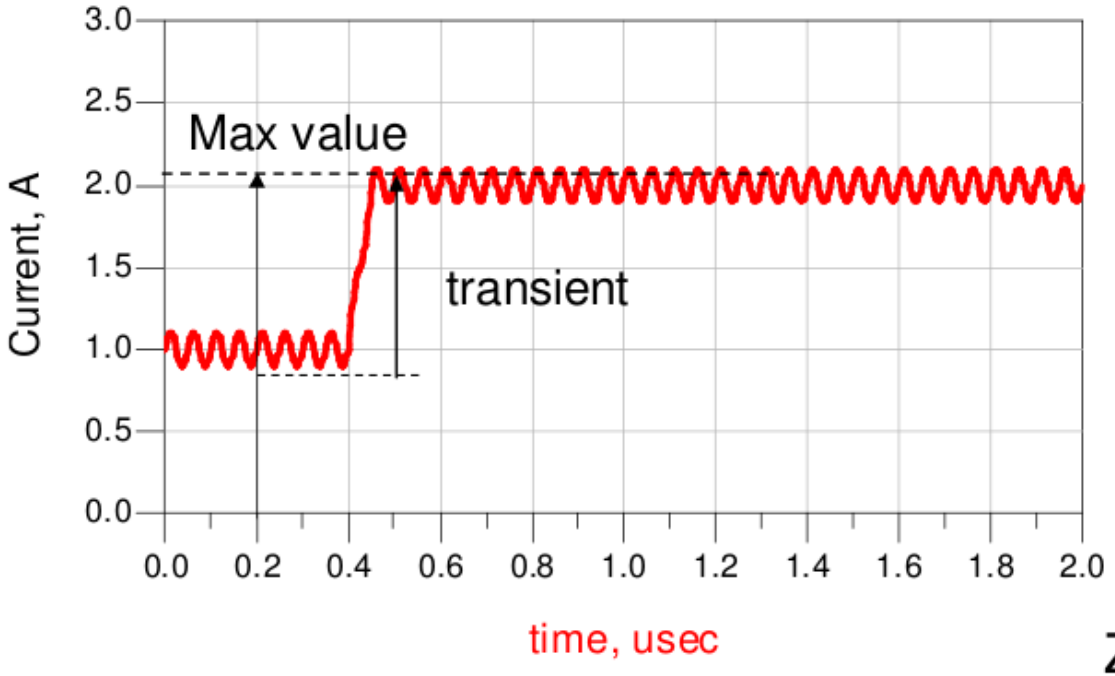
Dec 9, 2009

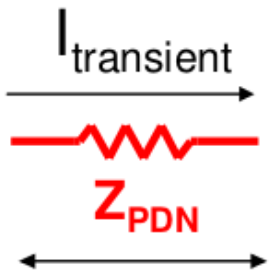
The Power Delivery Network



- All the interconnect from Voltage Regulator Module (VRM) to pads on the chip
- Purpose:
  - ✓ Provide stable voltage to chip pads from DC to > BW of the signals
  - ✓ Provide low impedance return path for signals
  - ✓ To help mitigate EMI emissions

1st Step: Estimate PDN Target Impedance





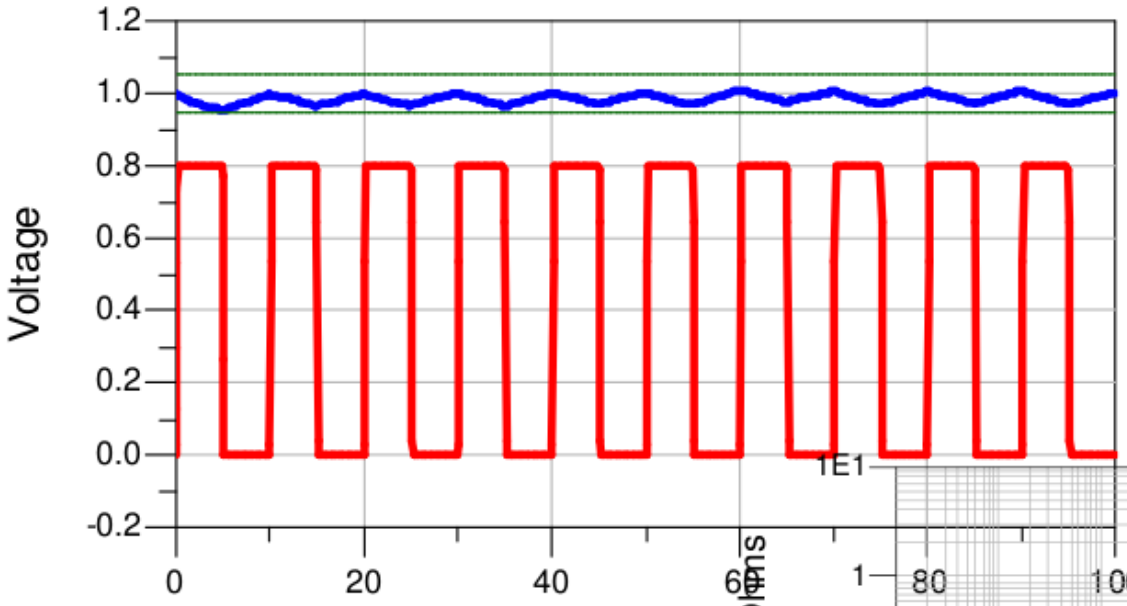
$$V_{PDN} = Z_{PDN} \times I_{transient}$$

$$Z_{PDN} < \frac{V_{dd} \times ripple}{I_{transient}} = Z_{target}$$

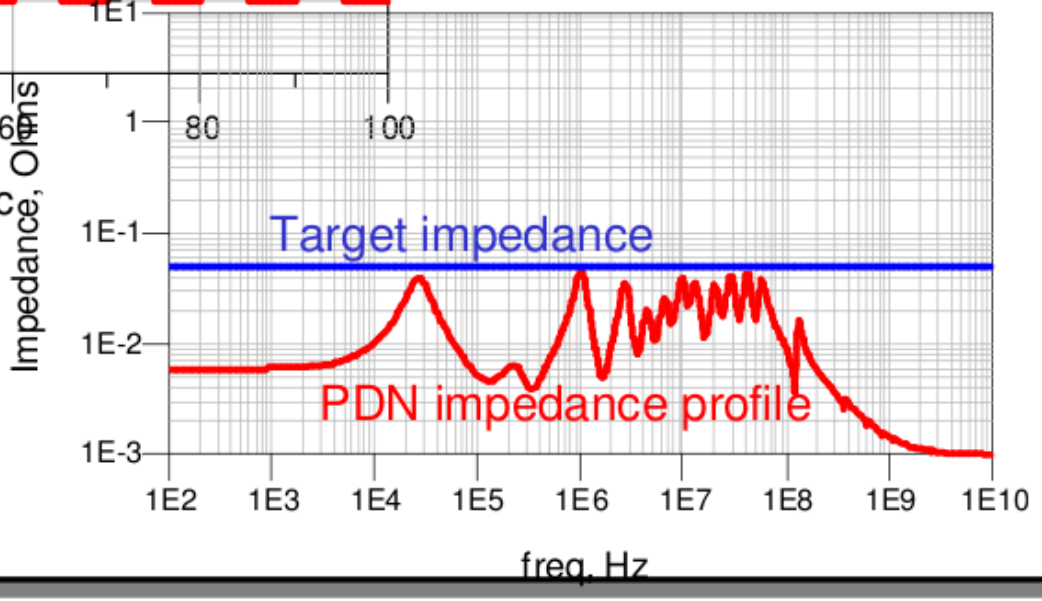
Example:
50 mV ripple noise
1 A transient current

Z_{PDN} ~ 50 mOhms

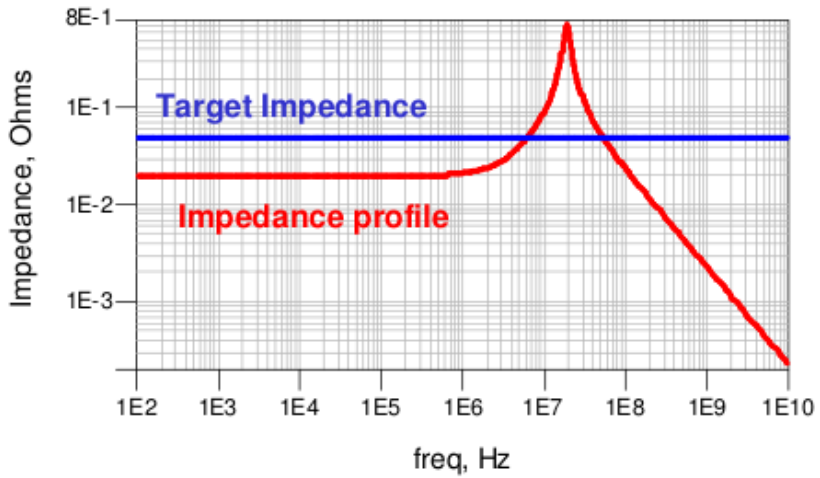
Goal: Keep PDN Impedance Below the Worst Case Target Impedance



1 A transient current
1 v Vdd
± 5% ripple spec
Target impedance ~ 50 mOhm

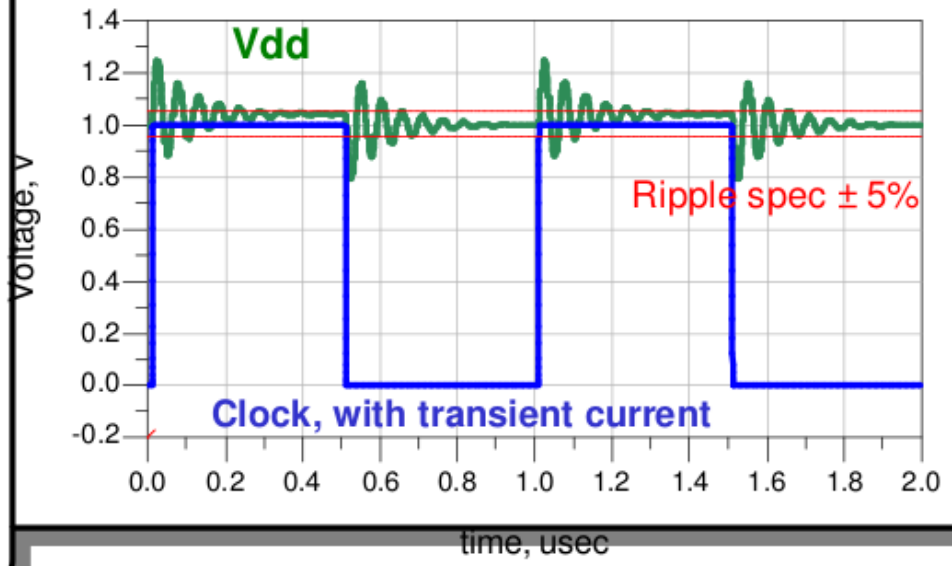


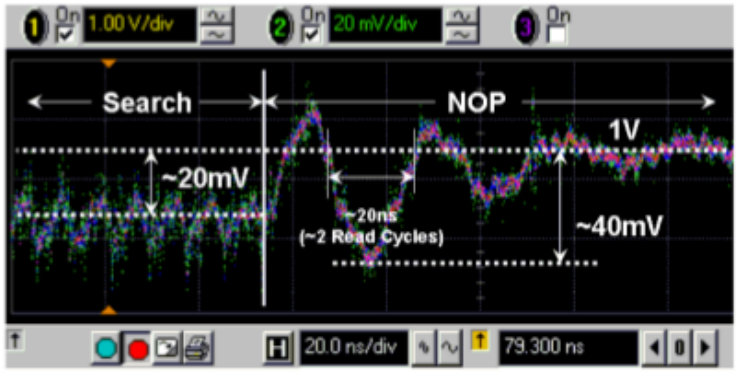
What if You Get it Wrong?



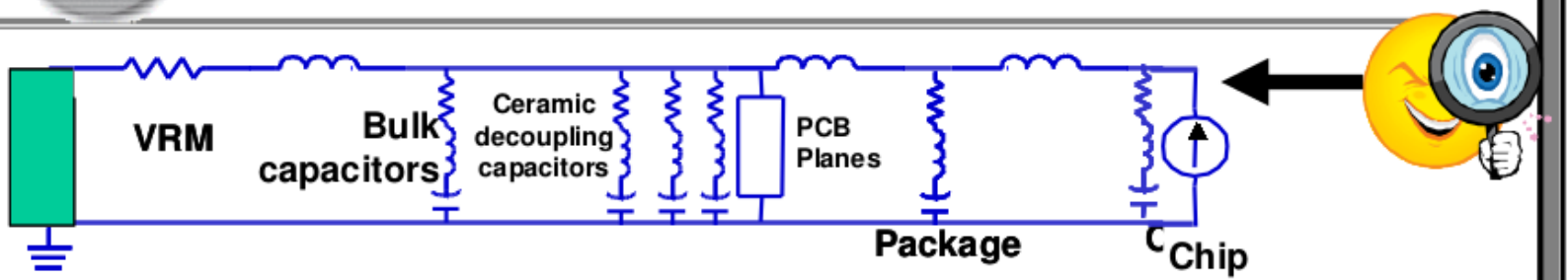
Golden Rule in PDN Design:

For robust PDN design, keep peak impedances below target impedance





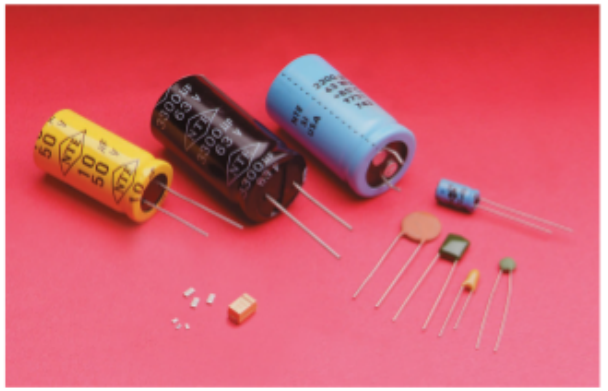
Elements of the PDN

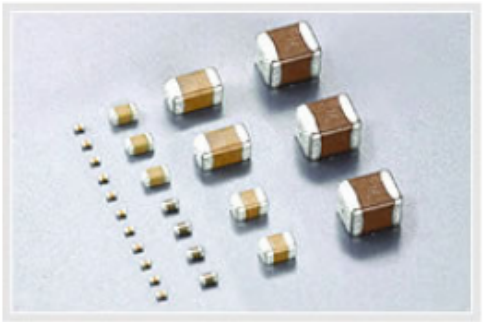


- On-chip capacitance
- Package lead inductance and on package decoupling (OPD) capacitors
- Power and ground planes
- MLCC (multi layer ceramic chip) capacitors
- Bulk tantalum, electrolytic capacitors
- The voltage regulator module (VRM)

How Many and What Value Capacitors to Use?

- ***It depends!***
- First order factors:
  - ✓ Target impedance
  - ✓ VRM equivalent inductance
  - ✓ On-die capacitance (ODC)
  - ✓ Package lead inductance, on-package decoupling (OPD) capacitance
  - ✓ Capacitor mounted inductance
- Second order factors
  - ✓ Power and ground plane capacitance
  - ✓ Planes' spreading inductance
  - ✓ Capacitor placement
- Risk reduction strategy



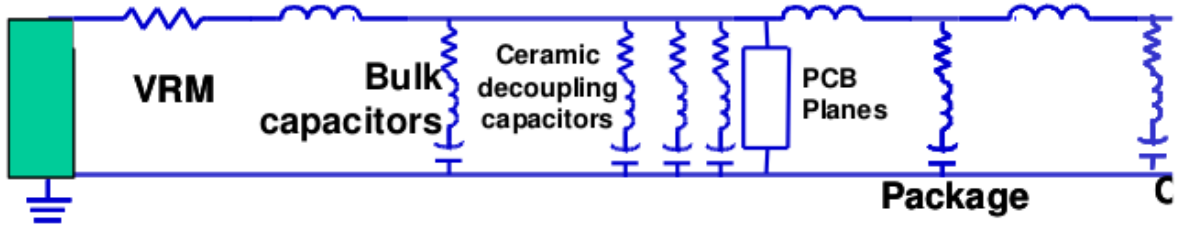


Approach #2

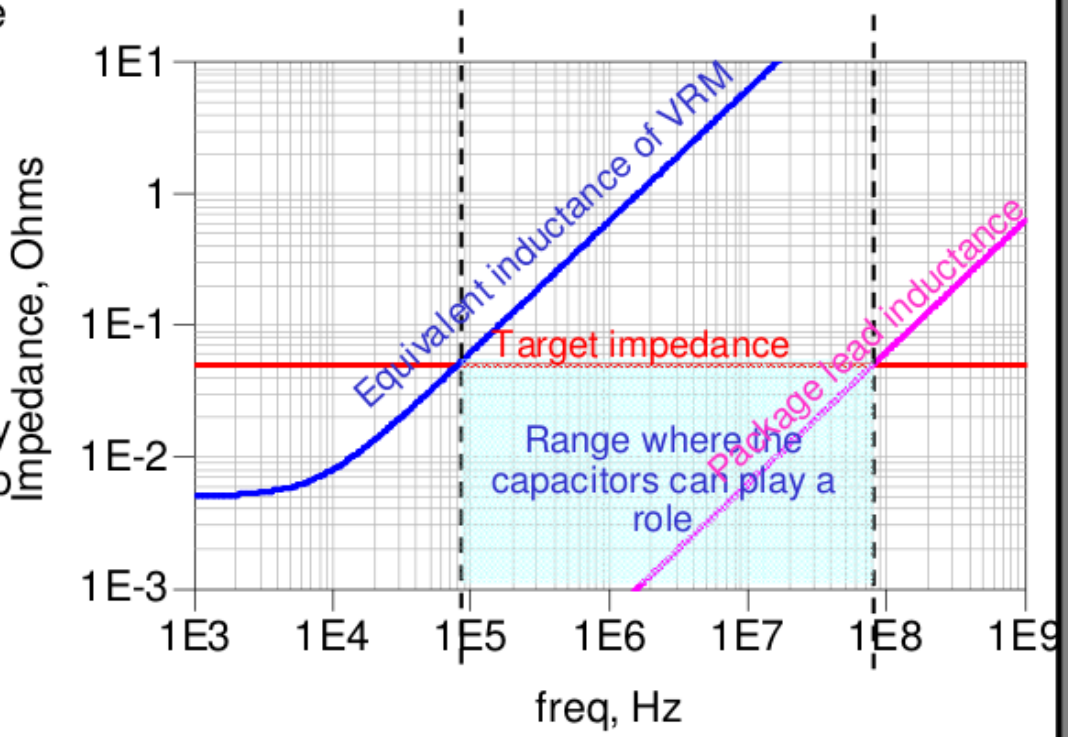
- Do your own analysis
  - ✓ Get the important starting information
  - ✓ Do a first order estimate
  - ✓ Add in second order factors
  - ✓ Do everything possible that is free
  - ✓ Use analysis tools to evaluate performance (SPICE, Agilent ADS, Altera PDN tool, Mentor PDN Analysis tool)
  - ✓ Select capacitor values and numbers based on impedance profile
  - ✓ Buy insurance by adding design margin
  - ✓ Use each design as an opportunity to move farther up the learning curve
  - ✓ The more you know, the luckier you get

Be The Signal

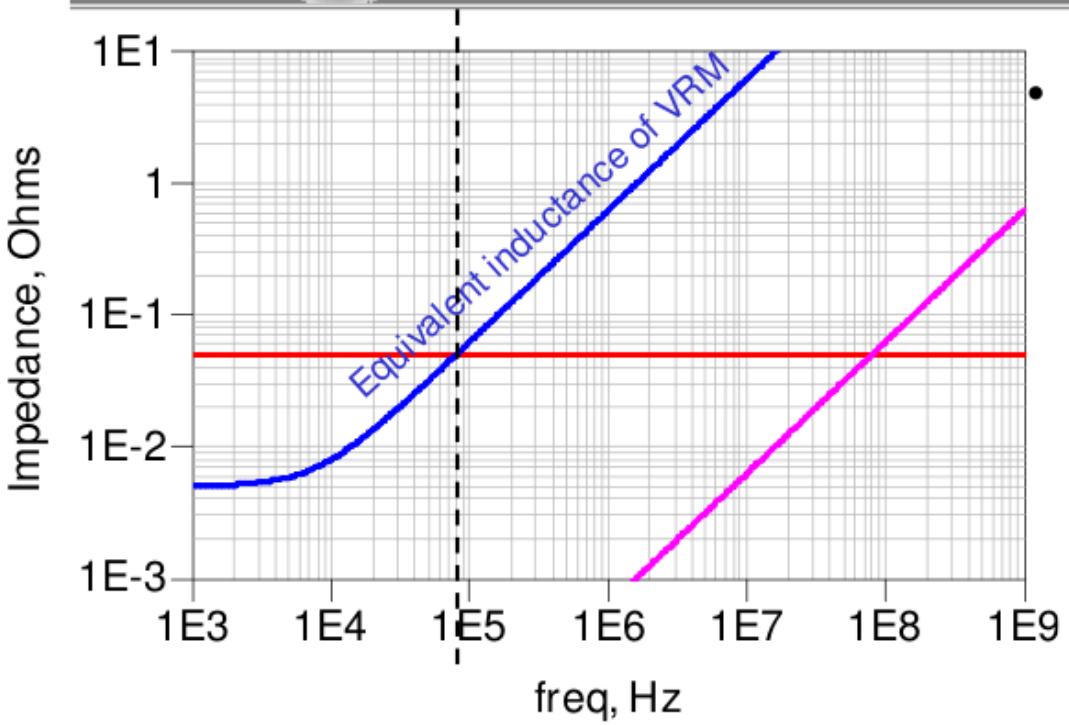
BEFORE You Can Intelligently Select Capacitor Values:



- ✓ Step 1: establish target impedance (based on transient current and noise spec)
- ✓ Step 2: establish the highest frequency where chip will see the board (based on package lead inductance)
- ✓ Step 3: establish the low frequency end where VRM is not able to keep the PDN impedance below the target impedance
- ✓ Defines 1st order goal: $Z_{cap} < 50$ mOhms, from 80 kHz to 80 MHz



Select Enough Bulk Capacitance for Low Frequency



- Select enough bulk capacitance so impedance is below target where regulator does not work

$$Z_C < Z_{target}$$

$$\frac{1}{(\omega C)} < Z_{target}$$

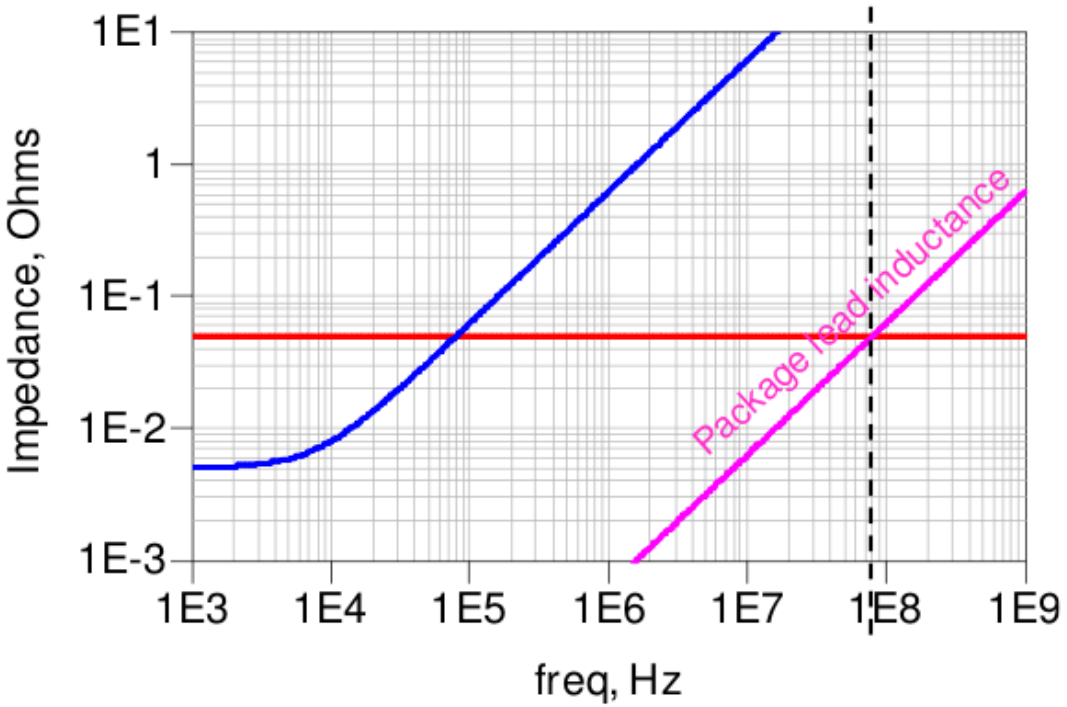
$$C > \frac{0.16}{f_{min} \times Z_{target}}$$

f_{min} = 80 kHz

Z_{target} = 50 mOhms

$$C > \frac{0.16}{0.08 \times 0.05} = 40uF$$

High Frequency Limit and Target Impedance Define Maximum Equivalent L



$$Z_C < Z_{target}$$

$$\omega L_{equiv} < Z_{target}$$

$$L_{equiv} < \frac{0.16 \times Z_{target}}{f_{max}[GHz]}$$

f_{max} = 80 MHz

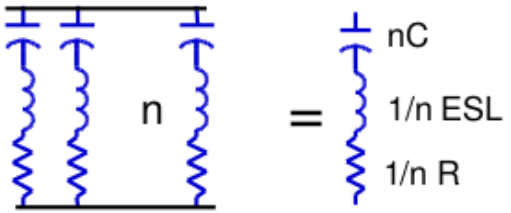
Z_{target} = 50 mOhms

$$L_{equiv} < \frac{0.16 \times 0.05}{0.08[GHz]} = 0.1nH$$

Comparable to the package lead inductance

First Order Analysis Summary

- Starting place
  - ✓ Target impedance = 50 mOhms
  - ✓ VRM frequency limit = 80 kHz
  - ✓ Package high freq limit = 80 MHz
- Enough capacitance for low freq = 40 uF
- Low enough inductance for high freq = 0.1 nH
  - ✓ Hard to achieve with 1 capacitor
  - ✓ Use multiple in parallel:



$$n = \frac{ESL}{L_{max}}$$

If ESL = 5 nH, n = 50

If ESL = 2 nH, n = 20

The ESL of the capacitors directly affects the cost of the PDN!

The ESL of the Capacitor Attach Affects the Minimum Number of Capacitors

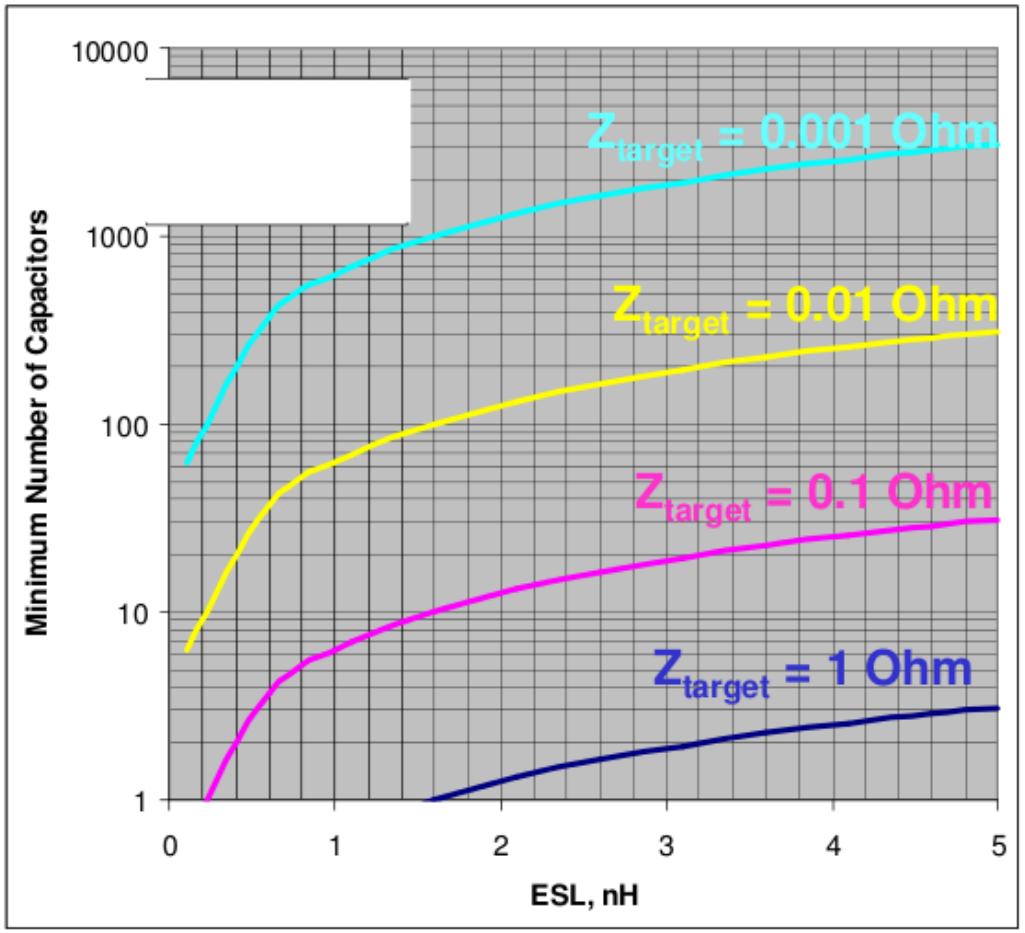
$$n > \frac{ESL \times f_{max}[GHz]}{0.16 \times Z_{target}}$$

Assume f_{max} = 100 MHz

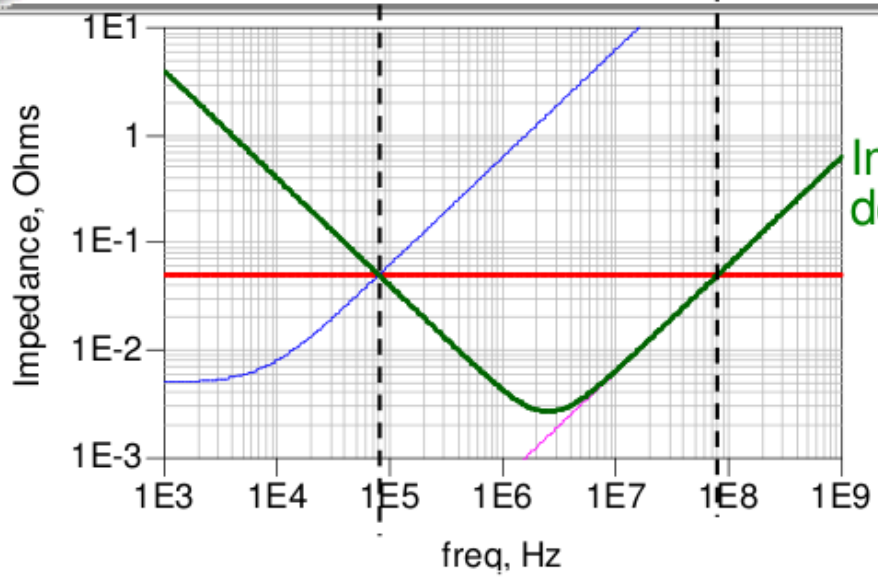
@ ~ 1¢/cap, this translates into cost savings per nH

The lower the ESL, the fewer the capacitor needed, the lower the cost

10 mOhm target, ESL ~ 1.5 nH cost of PDN caps = $1



Result of First Order Analysis



- Equivalent capacitance of 40 uF, equivalent inductance of 0.1 nH (20 @ 2 nH each)
  - ✓ Meets first order requirement!
  - ✓ We're done!
- …Welcome to the real world:
  - ✓ Interaction with the VRM
  - ✓ Interaction with the package L and on-die C
  - ✓ Interaction with the planes

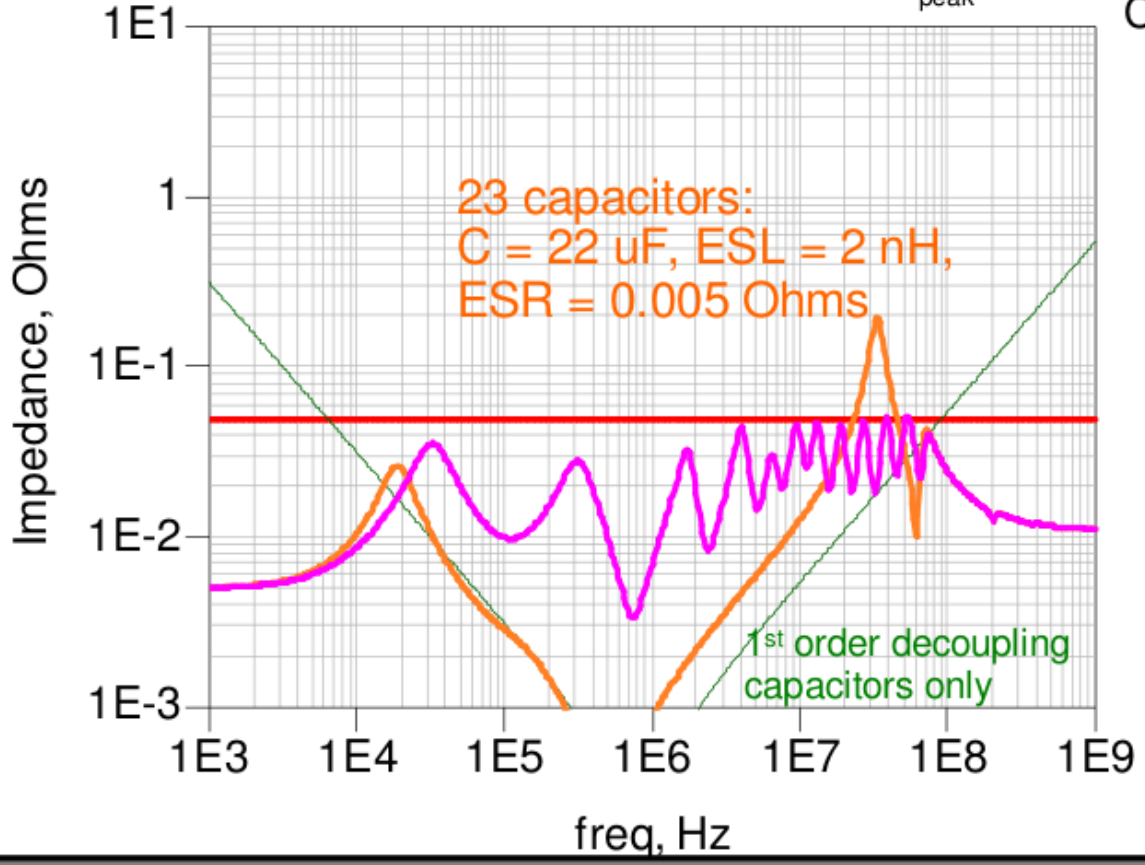
Leveraging the High ESR of Smaller Capacitors to Damp Parallel Resonances at High Frequency

Specific Case:
ODC = 100 nF
L_{pkg} = 0.1 nH
ESL = 2 nH

Estimated theoretical minimum number of capacitors: 20

Parallel resonant peak impedance

$$Z_{peak} \sim \frac{\left(\frac{1}{n}ESL + L_{pkg}\right)}{C_{chip}} \left(\frac{1}{\frac{1}{n}ESR + R_{pkg} + R_{chip}}\right)$$



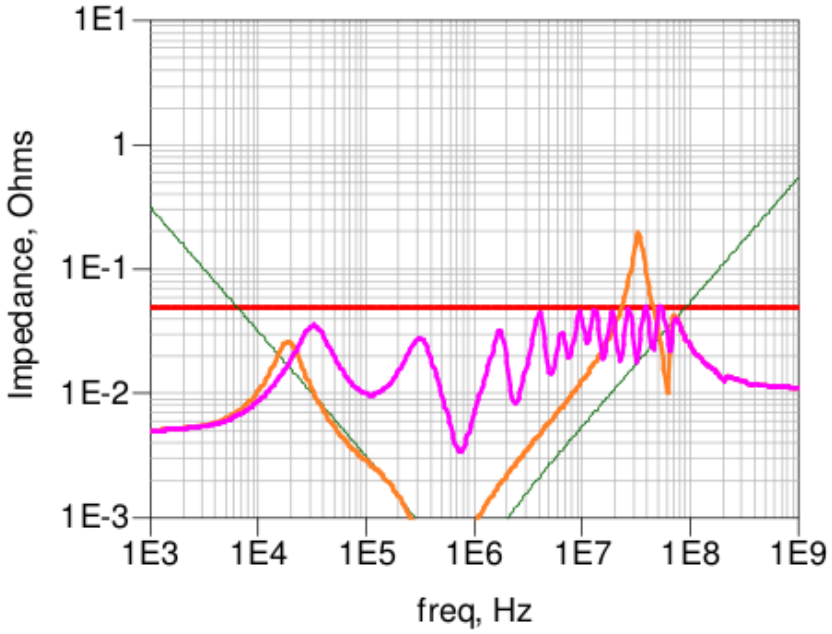
C nF	n
22000	1
2200	1
470	1
220	1
100	1
47	2
22	3
10	5
4.7	8
Total	**23**

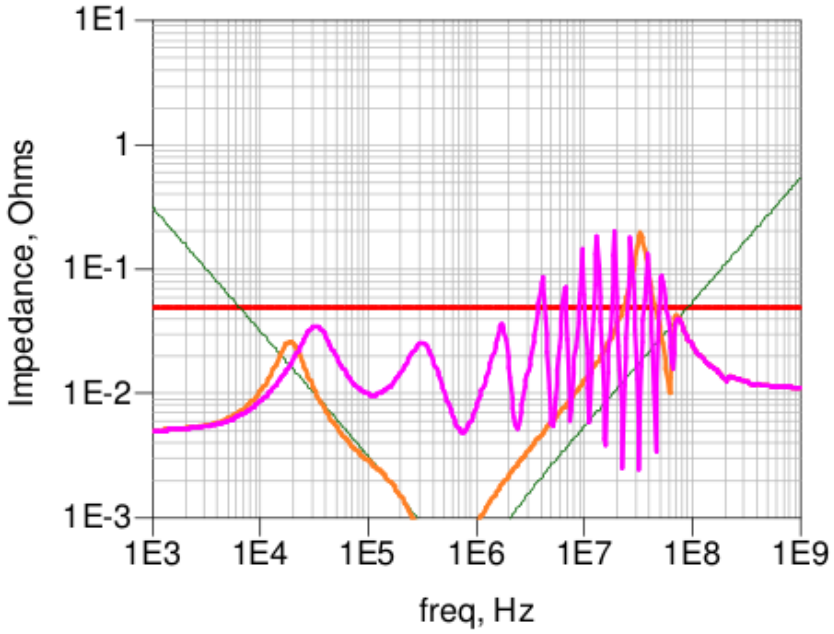
Impact of the Capacitor's ESR

Use multiple capacitor values:
1. Reduces peak impedance
2. Smaller C values have higher ESR

$$ESR \approx \frac{180m\Omega}{2.5^{\log(C)}}$$ C in nF

ESR = 0.005 Ohms





Strategy to Select Capacitor Values

- Use bulk capacitor for low frequency to minimize parallel impedance with VRM
- Minimize capacitor mounting inductance by design
  - ✓ Use thin dielectric between power and ground planes (reduces spreading inductance)
  - ✓ Use multiple vias per capacitor (reduces spreading inductance)
  - ✓ Stack power and ground cavity as close to surface as possible
  - ✓ Use shortest, widest surface traces between capacitors and vias
  - ✓ Know what it is!
- Include:
  - ✓ ESL, Target impedance, On-die capacitance, Package lead inductance
- Select smallest capacitor body size practical
  - ✓ Use simulation (free SPICE, Agilent ADS, Mentor HyperLynx PI, Altera PDN tool)
  - ✓ Start with largest capacitor value, 1 value per decade, then 3 values per decade
  - ✓ Adjust n to bring peak impedance below target impedance

Summary

- 1st order analysis
  - ✓ Enough capacitance for low frequency
  - ✓ Enough total number of capacitors for high frequency
  - ✓ Lower ESL is ALWAYS a good thing- fewer capacitors, more robust design
- 2nd order analysis
  - ✓ Optimize capacitor values to minimize parallel resonances
  - ✓ Leverage the higher ESR of small capacitors
- Other factors
  - ✓ When mounting inductance is small, spreading inductance in planes can be important- location matters
  - ✓ IDC capacitors (like x2y) can significantly reduce mounting inductance