# ADVANCED COMPACT MODEL FOR SHORT-CHANNEL MOS TRANSISTORS


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### Abstract

This paper introduces the advanced compact MOSFET (ACM) model, a physically based model of the MOS transistor, derived from the long-channel transistor model presented in (1). The ACM model is composed of very simple expressions, is valid for any inversion level, conserves charge and preserves the source-drain symmetry of the transistor. Short-channel effects are included using a compact and physical approach. The performance of the ACM model in benchmark tests demonstrates its suitability for circuit simulation.


### Introduction

The use of the CMOS VLSI technology has grown rapidly for a wide variety of applications, especially in battery-operated portable electronics. As a consequence, very complex analog/digital circuits must be integrated together, the circuits must be low-voltage operated and consume low power. This explosive growth of applications of CMOS circuits has increased the number of IC designers who work physically separated from the foundry. In this context, MOSFET models are the key element linking circuit design and fabrication.

This paper presents a compact MOSFET (ACM) model, which has been derived from a recent published (1) long-channel transistor model. The ACM model consists of simple and physically based continuous expressions, valid in all regions of operation, and verifies fundamental properties such as conservation of charge and the source-drain symmetry. It is also suitable for simulation of low-power and high-speed circuits since it describes fairly well the weak and moderate inversion regions and models accurately the intrinsic charges and (trans)capacitances of the MOS transistor.

### Fundamentals

The basic approximation of the ACM model is the linear dependence of the inversion charge density $Q_I'$ on the surface potential $\phi_S$ (1, 2). This assumption allows the model to be fully formulated in terms of the inversion charge densities at the source ($Q_{IS}'$) and drain ($Q_{ID}'$) ends of the channel. The relationship between the inversion charge density and the channel voltage ($V_C$) at any point of the channel is (1, 3)

$$V_P - V_C = \phi_t \left[ \frac{Q'_{IP} - Q'_I}{nC'_{OX}\,\phi_t} + ln\left( \frac{Q'_I}{Q'_{IP}} \right) \right] \qquad (1)$$

where $V_P$ is the pinch-off voltage, $Q'_{IP} = -nC'_{OX}\,\phi_t$ is the inversion charge density at pinch-off, n is the slope factor and $\phi_t$ is the thermal voltage. All voltages are referred to the local substrate, as in (4). Equation (1) is analogous to the "Unified Charge Control Model (UCCM)"(3).

### Short-channel effects

The DIBL (drain-induced barrier lowering) effect is represented by the parameter $\sigma$, which models the dependence of $V_P$ on both the drain and source voltages according to:

$$V_P(V_G, V_S, V_D) = V_{P0}(V_G) + \frac{\sigma}{n}(V_D + V_S) \qquad (2)$$

where $V_G$, $V_S$, and $V_D$ are the gate, source and drain voltages, respectively. $V_{P0}(V_G)$ is the pinch-off voltage for $V_D = V_S = 0$. The CLM (channel length modulation) is represented by a shrinkage of the channel length $\Delta L$ given by a conventional expression ( 3, 5).

The effect of carrier velocity saturation is included into the mobility model (2, 6) as

$$\mu_S = \frac{\mu}{1 + \frac{\mu}{v_{lim}} \frac{d\phi_S}{dx}} \qquad (3)$$

where $v_{lim}$ is the saturation velocity and $\mu$ is the mobility of the long-channel device, which has been assumed to be a function of $V_G$ only.

The drain current including velocity saturation is given by

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$$I_D = \frac{\mu W_{eff}}{C'_{ox} L_{eq}} \frac{1}{1+\frac{|Q'_F - Q'_R|}{Q'_A}} \frac{Q'^2_F - Q'^2_R}{2n} \quad (4.a)$$

where, $Q'_{F(R)} = Q'_{IS(D)} - nC'_{OX}\phi_t$, $L_{eq} = L_{eff} - \Delta L$, $L_{eff}$ and $W_{eff}$ are the effective channel length and width and

$$Q'_A = nC'_{ox} L_{eq} \frac{v_{lim}}{\mu} \quad (4.b)$$

For the purpose of electrical simulation, the factor $|Q'_F - Q'_R|/Q'_A$ in equation (4.a) is replaced with a continuous and smooth function to avoid discontinuities in the derivatives of the drain current around $V_{DS} = 0$.

**Operation in saturation**

Assuming that in the saturation region the carriers flow at saturation velocity, the minimum amount of charge density ($Q'_{IDSAT}$) required to sustain the current is given by

$$Q'_{IDSAT} = -\frac{I_D}{W_{eff} v_{lim}}. \quad (5)$$

Equation (5) is a physical definition for saturation that, together with (4), allows one to calculate the value of the charge density associated with the drain that corresponds to the onset of saturation

$$Q'_{IDSAT} = Q'_{IS} - nC'_{OX}\phi_t - Q'_A\left[1-\sqrt{1-\frac{2(Q'_{IS} - nC'_{OX}\phi_t)}{Q'_A} + \frac{(nC'_{OX}\phi_t)^2}{Q'^2_A}}\right]. \quad (6)$$

$Q'_{IDSAT}$ is a function of the source and gate voltages, through $Q'_{IS}$, and of the channel length, through $Q'_A$. Fig.1 illustrates the variation of the ratio $Q'_{IDSAT}/Q'_{IS}$ with respect to $Q'_{IS}$ normalized to the charge density at pinch-off for three values of ε, a parameter associated with the velocity saturation phenomenon.

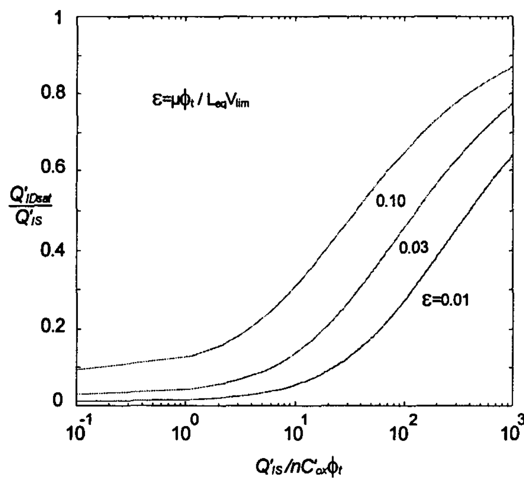


Fig.1. Drain charge density at the onset of saturation versus source charge density for different values of ε.

From the charge-voltage relationship given by (1), one can readily calculate $V_{DSSAT}$, the drain-to-source voltage for which the charge density at the drain end corresponds to the onset of saturation.

**Intrinsic charges and (trans)capacitances**

To calculate the total inversion charge, the channel is split into the saturated and non-saturated regions. In the saturated region the inversion charge density is assumed to be constant; therefore, the inversion charge is given by

$$Q_I = W_{eff} \int_0^{L_{eq}} Q'_I dx + W_{eff} \Delta L Q'_{IDSAT}, \quad (7)$$

where $dx$ can be written as

$$dx = -\frac{\mu W_{eff}}{nC'_{ox} I_D}\left(Q'_I - nC'_{ox}\phi_t + \frac{I_D}{W_{eff} v_{lim}}\right) dQ'_I. \quad (8)$$

After integration, the total inversion charge is

$$Q_I = W_{eff} L_{eq}\left(\frac{2}{3}\frac{q_f^2 + q_f q_r + q_r^2}{q_f + q_r} + nC'_{ox}\phi_t - \frac{I_D}{W_{eff} v_{lim}}\right) + W_{eff} \Delta L Q'_{IDSAT} \quad (9)$$

where

$$q_{f(r)} = Q'_{F(R)} + \frac{I_D}{W_{eff} v_{lim}} \quad (10)$$

Using the same approach, the depletion charge ($Q_B$) and the charges at the gate ($Q_G$), drain ($Q_D$) and source ($Q_S$) terminals are calculated:

$$Q_B = -\frac{n-1}{n} Q_I - W_{eff} L_{eq} \frac{\gamma^2 C'_{ox}}{2(n-1)}, \quad (11)$$

$$Q_G = -Q_B - Q_I, \quad (12)$$

$$Q_D = \frac{W_{eff} L^2_{eq}}{L_{eff}}\left(\frac{2}{15}\frac{3q_r^3 + 6q_r^2 q_f + 4q_r q_f^2 + 2q_f^3}{(q_f + q_r)^2} + \frac{nC'_{ox}\phi_t - \frac{I_D}{W_{eff} v_{lim}}}{2} + W_{eff}\frac{L^2_{eff} - L^2_{eq}}{2L_{eff}} Q'_{ID}\right), \quad (13)$$

$$Q_S = Q_I - Q_D. \quad (14)$$

The expressions described above for the charges are similar to those reported in (6).

The (trans)capacitances are defined as

$$C_{kj} = -\frac{\partial Q_k}{\partial V_j}, \; C_{jj} = \frac{\partial Q_j}{\partial V_j} \quad (19)$$

where $Q_k$ and $Q_j$ are any of the charges $Q_G$, $Q_B$, $Q_S$ or $Q_D$ and $V_j$ is any of the potentials $V_G$, $V_B$, $V_S$ or $V_D$. The expressions above define 16 (trans)capacitances from which a maximum set of 9 are independent.

Applying the definition (19) to the formulas previously derived for the total charges, we found the expressions for the 9 independent (trans)capacitances in Table I, which includes the effects of both DIBL and velocity saturation. In Table I, $g_{ms}$, $g_{md}$ and $g_{mg}$ are the source, drain and gate transconductances, respectively, and $g_{mb} = g_{ms} - g_{md} - g_{mg}$ is the bulk transconductance.

The partial derivatives of $n$, $\Delta L$ and of the channel length modulation term of the total charges have been neglected in the derivation of the expressions in Table I.

### Benchmark tests

Papers have been published suggesting benchmarks (7, 8) to evaluate MOSFET models. This section presents a few simulation examples run on SMASH (9) which demonstrate the suitability of the ACM model to some of the tests proposed in (7, 8).

In Fig. 2 a comparison is shown between the values of the gate transconductance-to-current ratio ($g_{mg}/I_D$) evaluated from ACM and BSIM 3v3 models, versus the normalized drain current $i_d = I_D/I_S$, with $I_S = (W_{eff}/L_{eff})\mu n C'_{ox}\phi_t^2/2$. It is noticeable that, according to BSIM 3v3 model, the ratio $g_{mg}/I_D$ tends to be constant in weak inversion, which is inconsistent with the physical behavior of the device. The correct behavior of $g_{mg}/I_D$ in weak inversion can also be verified from the plot $g_{mg}/I_D$ versus $V_G$ for several values of $V_S$. The top of the curves must approach the reciprocal of the thermal voltage as $V_S$ increases. This test, known as the Gummel treetop test (8), was applied to the ACM model and the results are shown in Fig. 3.

The circuit in Fig. 4(a) is employed for the Gummel symmetry test (8). This test is used to show the symmetry of forward and reverse modes of operation and the continuity, around the origin, of the drain current and charges as well as their derivatives. Fig. 4(b) shows the first and second order derivatives of the drain current, both continuous and symmetric around $V_{DS}=0$.

Finally, Fig. 5 shows the dependence of $C_{gd}$, and $C_{gs}$ on the channel length. Due to DIBL $C_{gd}$ becomes negative for the transistor whose channel length is 0.8μm, the minimum value for this technology

### Conclusion

The ACM long-channel model (1) has been revised for the inclusion of short-channel effects. Expressions for the drain current, total inversion, depletion, gate, drain, source charges and intrinsic (trans)capacitances have been presented considering the effects of DIBL, CLM and velocity saturation. Circuit simulations run on SMASH with ACM model demonstrated that the gate transconductance is continuous, smooth and presents the proper behavior in weak inversion. The first and second order derivatives of the drain current are symmetrical and continuous around $V_{DS}=0$. The MOSFET capacitances are continuous and vary smoothly with the channel length. The simplicity of the ACM model together with its robustness to severe tests make it a valuable choice for the simulation of MOS circuits.

TABLE I
INTRINSIC (TRANS)CAPACITANCES

| Variable | Expression |
|---|---|
| $C_{gs}$ | $C_{gso} - \frac{\sigma}{n}\left(C_{gso} + C_{gdo}\right) - \frac{F_1}{3n}\frac{L_{eq}}{v_{\lim}} g_{ms}$ |
| $C_{gd}$ | $C_{gdo} - \frac{\sigma}{n}\left(C_{gso} + C_{gdo}\right) + \frac{F_1}{3n}\frac{L_{eq}}{v_{\lim}} g_{md}$ |
| $C_{gb}$ | $\frac{n-1}{n}\left(C_{ox} - C_{gso} - C_{gdo}\right) + 2\frac{\sigma}{n}\left(C_{gso} + C_{gdo}\right) + \frac{F_1}{3n}\frac{L_{eq}}{v_{\lim}} g_{mb}$ |
| $C_{dd}$ | $\frac{L_{eq}}{L_{eff}}\left[C_{ddo} + \frac{\sigma}{n}\left(C_{dso} - C_{ddo}\right) + F_2\frac{L_{eq}}{v_{\lim}} g_{md}\right]$ |
| $C_{ds}$ | $\frac{L_{eq}}{L_{eff}}\left[C_{dso} + \frac{\sigma}{n}\left(C_{ddo} - C_{dso}\right) + F_2\frac{L_{eq}}{v_{\lim}} g_{ms}\right]$ |
| $C_{dg}$ | $\frac{L_{eq}}{L_{eff}}\left[\frac{\left(C_{ddo} - C_{dso}\right)}{n} - F_2\frac{L_{eq}}{v_{\lim}} g_{mg}\right]$ |
| $C_{db}$ | $\frac{L_{eq}}{L_{eff}}\left[\frac{\left(n-1-2\sigma\right)}{n}\left(C_{ddo} - C_{dso}\right) - F_2\frac{L_{eq}}{v_{\lim}} g_{mb}\right]$ |
| $C_{bs}$ | $\left(n-1\right)C_{gs}$ |
| $C_{bd}$ | $\left(n-1\right)C_{gd}$ |
| $C_{ox}$ | $W_{eff} L_{eq} C'_{ox}$ |
| $F_1(q_f, q_r)$ | $1 - 2\frac{q_f^2 + q_f^2}{\left(q_f + q_r\right)^2}$ |
| $F_2(q_f, q_r)$ | $\frac{2}{15}\frac{2q_f^3 + 14q_f^2 q_r + 11q_f q_r^2 + 3q_r^2}{\left(q_f + q_r\right)^3} - \frac{1}{2}$ |
| $C_{gs(d)o}$ | $C_{ox}\left(1 - \frac{q_{r(f)}^2}{\left(q_f + q_r\right)^2}\right)\left(1 + \frac{nC'_{ox}\phi_t}{Q'_{F(R)}}\right)$ |
| $C_{ddo}$ | $nC_{ox}\frac{2}{15}\frac{3q_r^3 + 9q_r^2 q_f + 8q_r q_f^2}{\left(q_f + q_r\right)^3}\left(1 + \frac{nC'_{ox}\phi_t}{Q'_R}\right)$ |
| $C_{dso}$ | $-nC_{ox}\frac{2}{15}\frac{2q_f^3 + 6q_f^2 q_r + 2q_f q_r^2}{\left(q_f + q_r\right)^3}\left(1 + \frac{nC'_{ox}\phi_t}{Q'_F}\right)$ |

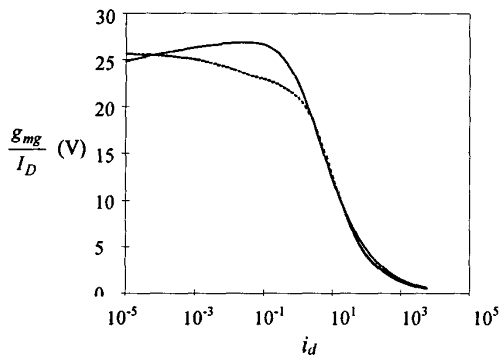


Fig.2. Comparison between gate transconductance-to-current ratio evaluated from the ACM (——) model and from BSIM 3v3 (- - - -)

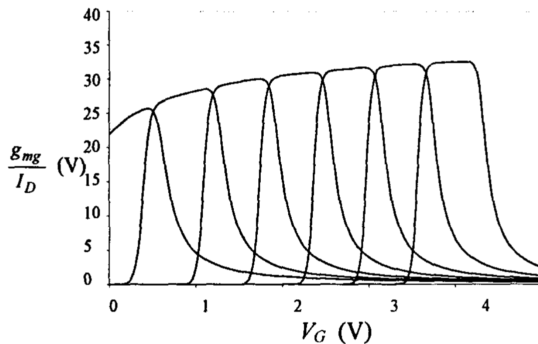


Fig. 3. Transconductance-to current ratio versus gate voltage with the source voltage varying from 0 to 3V in steps of 0.5V.


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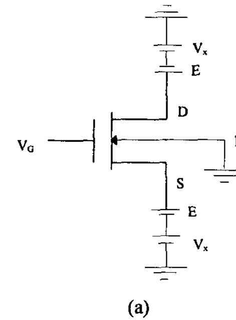


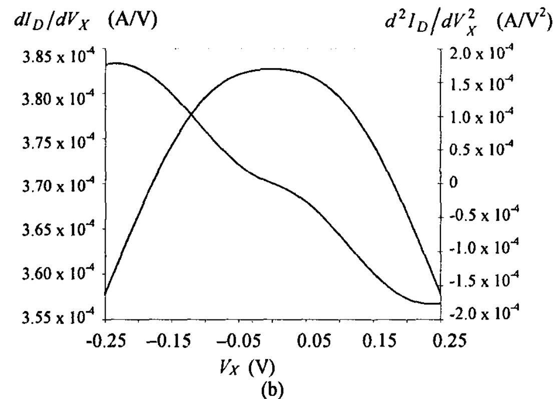


Fig.4. (a) Circuit for testing the symmetry of the model at $V_{DS} = 0V$.
(b) Simulation results using the ACM model

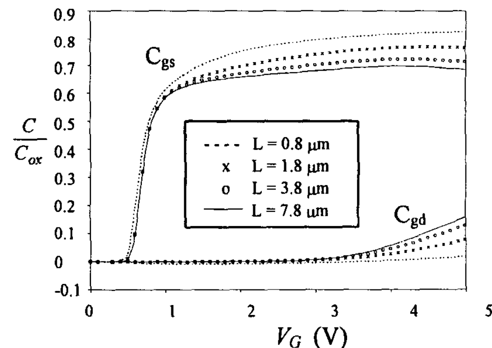


Fig.5 – Normalized $C_{gs}$ and $C_{gd}$ versus $V_G$ for channel-lengths varying from 0.8μm to 7.8μm. $V_G$=$5V$ and $V_S$=$V_B$=$0V$.

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