Design of RF CMOS Low Noise Amplifiers Using a Current Based MOSFET Model

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ABSTRACT
This paper presents a design methodology for RF CMOS Low Noise Amplifiers (LNA). This methodology uses a current–based MOSFET model, which allows a detailed analysis of an LNA for all MOSFET's inversion regions. Design equations, including the induced gate noise in MOS devices are also presented and a design example with simulation results is shown.

Categories and Subject Descriptors
B.7.1 **[ASIC]**: Circuit design and simulation, RF integrated circuits, low noise amplifiers.

General Terms
Theory, design.

Keywords
CMOS, RF, LNA, noise.

1. INTRODUCTION
RF integrated circuit design is increasingly taking advantage of the aggressive scaling of submicrometer CMOS technologies that make possible the integration of complete telecommunication systems in a single chip. Although several real chips containing RF parts have been appeared in the last few years, the design of RF CMOS integrated circuits remains a challenge due to strong constraints in power consumption and noise.

The first stage of a receiver is typically a low noise amplifier (LNA), whose main function is to provide enough gain for subsequent stages, [1], while adding as little noise as possible. An LNA should also accommodate large signals without distortion, and frequently must also present a specific impedance, such as 50 Ω to the input source. All these functions must be performed with low power consumption.

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Several authors have presented design methodologies for MOS low noise amplifiers [1-2]. However, in their designs, the transistors always operate in strong inversion. Doing so, they don't take the advantages of weak and moderate inversion operation, such as a higher g_m/I_D. A design in moderate inversion is presented in [3], but the MOSFET model is very complex.

In this paper we propose a new methodology for the LNA design, using a current based MOSFET model [4], which is valid from weak to strong inversion regions including moderate inversion.

This modeling permits the design of the LNA in moderate inversion, which appears to provide a good tradeoff between noise and power consumption.

2. MOSFET MODEL
The dc and ac operations as well as the noise model of the MOS transistor can be described in terms of the different charges stored in the device and more specifically of the inversion mobile charge density Q'_I, evaluated at the source and drain ends of the channel and defined as Q'_{IS} and Q'_{ID}, respectively [4]. In this model, the drain current I_D is split into the difference between a forward current I_F and a reverse current I_R [4]

$$I_D = I_F - I_R = I(V_G, V_S) - I(V_G, V_D) \tag{1}$$

where

$$I_{F(R)} = \mu n \cdot C'_{ox} \frac{\phi_t^2}{2} \frac{W}{L} \left[\left(\frac{Q'_{IS(D)}}{nC'_{ox}\phi_{tt}} \right)^2 - 2 \frac{Q'_{IS(D)}}{nC'_{ox}\phi_{tt}} \right] \tag{2}$$

μ is the mobility, n is the slope factor, C'_{ox} is the oxide capacitance per unit area, ϕ_t is the thermodynamic potential, W is the transistor width, and L the transistor length.

Expression *(2)* can be rewritten in the form:

$$\sqrt{1 + i_{f(r)}} - 1 = -\frac{Q'_{IS(D)}}{nC'_{ox}\phi_t} \tag{3}$$

where

$$i_{f(r)} = \frac{I_{F(R)}}{I_s} \tag{4}$$

is the forward (reverse) normalized current and

$$I_S = \mu.n.C'_{ox}\frac{\phi_t^2}{2}\frac{W}{L} \tag{5}$$

is the normalization current [4].

The normalized currents i_f and i_r characterize the state of inversion of the channel at the source and at the drain, respectively. They can, therefore, be used to define different modes of operation. The normalized forward and reverse currents are also related to the ac small-signal parameters. The source and drain transconductances g_{ms} and g_{md} are given by

$$g_{ms(d)} = \frac{2I_s}{\phi_t}\left(\sqrt{1+i_{f(r)}}-1\right). \tag{6}$$

The gate transconductance is then simply calculated from [2, 3] as

$$g_m = \frac{1}{n}\left(g_{ms} - g_{md}\right) \tag{7}$$

In saturation, $i_f >> i_r$ and, therefore, $g_{ms} >> g_{md}$ resulting in the gate transconductance becoming simply proportional to the source transconductance $g_m = g_{ms}/n$.

The small signal capacitances are also expressed in terms of the normalized currents [4], the gate to source and gate to bulk capacitances, in saturation are, respectively

$$C_{gs} = WLC'_{ox}\frac{2}{3}\left(\sqrt{1+i_f}-1\right)\frac{\sqrt{1+i_f}+2}{\left(\sqrt{1+i_f}+1\right)^2} \tag{8}$$

$$C_{gb} = \left(\frac{n-1}{n}\right)\left(WLC'_{ox} - C_{gs}\right). \tag{9}$$

Finally, the inversion charge in saturation is

$$Q_I = -C_{ox}n\phi\left[\frac{2}{3}\left(\sqrt{1+i_f}+1-\frac{\sqrt{1+i_f}}{\sqrt{1+i_f}+1}\right)-1\right]. \tag{10}$$

An important figure of merit for the MOS transistor is the intrinsic cutoff frequency, defined as the frequency value at which the short-circuit current gain in the common-source configuration drops to 1. An approximation for the intrinsic cutoff frequency has been presented in [4] as

$$f_T \cong \frac{\mu\phi_t}{2\pi L^2}2\left(\sqrt{1+i_f}-1\right). \tag{11}$$

3. HIGH-FREQUENCY NOISE MODEL

3.1. Noise Sources in the MOS Transistor

The different noise sources in the MOS transistor are shown in figure 1 together with their power spectral densities (PSD). They include: the noise at drain constituted by the channel thermal noise and the flicker noise and the terminal gate resistance thermal noise. The flicker noise mainly affects the low-frequency performance of the device and can be ignored at high-frequency. In addition to the channel thermal noise at the drain, at high-frequency the local noise sources within the channel capacitively couple the gate and generate an induced gate noise [4].

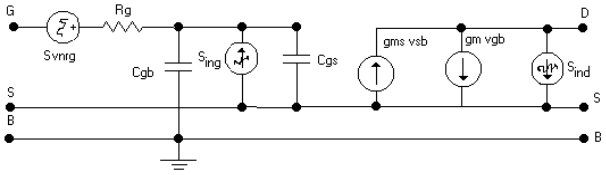

Figure 1. Noise sources in the MOS transistor in saturation.

3.2. Channel Thermal Noise

Although all the noise sources contribute to the total noise at high-frequency, the dominant contribution still comes from the channel thermal noise, which can be expressed as [4]

$$S_{id} = -\frac{4KT\mu Q_I}{L^2}, \tag{12}$$

where K is the Boltzmann constant, T the absolute temperature, and Q_I the total inversion charge. Equation (12) is valid from weak to strong inversion and includes the contribution of shot noise in weak inversion [4].

From (12), it follows that the MOSFET thermal noise is the same as the one produced by a conductance G_{nch} whose value is [4]

$$G_{nch} = \frac{\mu|Q_I|}{L^2} = g_{ms}\frac{Q_I}{Q'_{IS}WL}. \tag{13}$$

(13) can be expressed in terms of the inversion level and becomes, in saturation,

$$G_{nch} = g_{ms}\left\{\frac{1}{\sqrt{1+i_f}+1}\left[\frac{2}{3}\left(\sqrt{1+i_f}-1\right)+1\right]\right\}. \tag{14}$$

Equation (12) together with (6), (10), (13) and (14) allows S_{id} to be written a

$$S_{id} = 4KT\frac{W}{L}\mu_0 nC'_{ox}\phi_t\left\{\frac{\sqrt{1+i_f}-1}{\sqrt{1+i_f}+1}\left[\frac{2}{3}\left(\sqrt{1+i_f}-1\right)+1\right]\right\} \tag{15}$$

This very compact expression, a function of the normalized currents i_f and i_r, is valid for any bias set of voltages. Figure 2 shows the behavior of the thermal noise PSD as the inversion level varies.

3.3. Induced Gate Noise

At high-frequency, the local channel voltage fluctuations due to thermal noise couple to the gate through the oxide capacitance and cause an induced gate noise current to flow [2, 5]. In saturation, most of the channel charge is located on the source side and, hence, this noise current can be modeled by a single noisy current source S_{ing} connected in parallel with C_{gs}, with a PSD given by [2]

$$S_{ing} = 4KT\delta\frac{(\omega C_{gs})^2}{5g_{ms}} \tag{16}$$

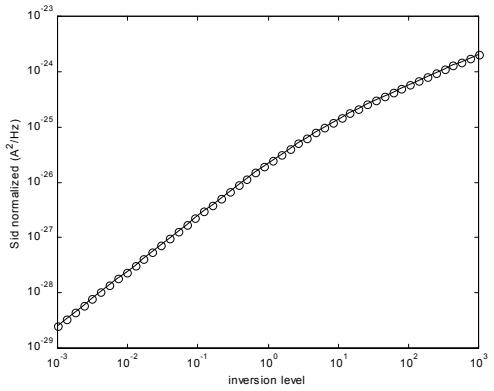

Figure 2. Power spectral density of thermal noise in function of the inversion level

where δ is defined as a factor of excess induced gate noise and is assumed to be equal to 4/3 [2].

To understand how the induced gate noise affects the device when the inversion condition changes, it can be expressed in function of the inversion level. With the aid of equations (6) and (8), the PSD of induced gate noise is written as

$$S_{ig} = \frac{8}{45} KT \frac{\delta \cdot \omega^2 \cdot W \cdot L^3 \cdot C'_{ox}}{\mu n \phi_t} \left[\frac{\left(\sqrt{1+i_f} - 1\right) \cdot \left(\sqrt{1+i_f} + 2\right)^2}{\left(\sqrt{1+i_f} + 1\right)^4} \right] \quad (17)$$

Figure 3 shows the behavior of the PSD of induced gate noise as the inversion level varies for transistors with different W/L ratios, operating at 2.5 GHz.

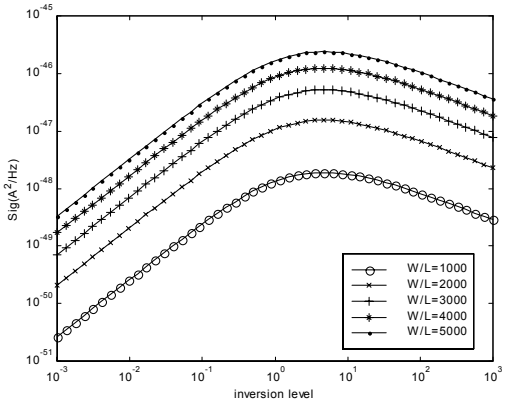

Figure 3. Power spectral density of induced gate noise in function of the inversion level for several W/L values for frequency of 2.5 GHz.

Since the induced gate noise and the channel thermal noise have the same physical origin, the two noise sources are partially correlated, with a correlation factor given in [2, 5].

The correlation can be treated by expressing the gate noise as the sum of two components, the first of which is fully correlated with the channel noise, and the second of which is uncorrelated with the channel noise [5].

4. LNA ANALYSIS

The LNA design involves tradeoffs between many figures of merit, such as gain, noise, power, impedance matching, stability, and linearity. In this section we proceed the analysis of the LNA which the schematic is shown in figure 4.

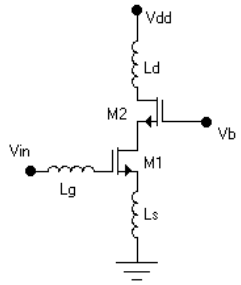

Figure 4. Simplified schematic of a cascode LNA with inductive source degeneration.

4.1. Impedance Matching

The amplifier of figure 4 has been analyzed by several authors [1-3], however in those analysis the body bias and the capacitance C_{gb} are always neglected. Although this approach leads to good results when the transistors operate in strong inversion, that is not the case if they are operating in moderate or weak inversion. So we must consider C_{gb} to derive the input impedance of the amplifier. The small signal model of the amplifier is shown in figure 5.

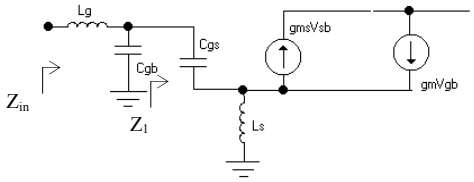

Figure 5. Small signal model for the cascode LNA

From the analysis of the circuit in figure 5, and after some approximations

$$Z_1 = \frac{1}{\omega^2 L_s C_{gs} g_m} \cdot \frac{1}{1 + \frac{j\omega C_{gs}}{\omega^2 L_s C_{gs} g_m}} \quad (18)$$

which can be viewed as the parallel of a resistor R with the capacitance C_{gs}.

The circuit of figure 5 simplifies to the one in figure 6.

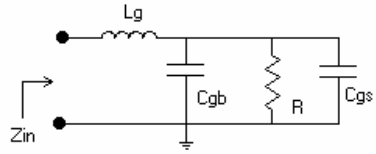

Figure 6. Simplified small signal model of figure 5

The analysis of the circuit in figure 6 is straightforward and yields to

$$Z_{in} = \frac{R}{1+\omega^2 R^2 C^2} + j\omega \frac{\left[L_g - R^2 C\left(1-\omega^2 L_g C\right)\right]}{1+\omega^2 R^2 C^2} \quad (19a)$$

where R and C are given by

$$R = \frac{1}{\omega^2 L_s C_{gs} g_m} \quad (19b)$$

$$C = C_{gs} + C_{gb}\,. \quad (19c)$$

Since we are dealing with a narrow band LNA, we only need to provide impedance matching in this narrow bandwidth. The matching is achieved simply by making the real part of (19) equal to the source resistance and its imaginary part equal to zero. The matching conditions are set by the proper choice of the inductances of L_s and L_g. L_s is used to make the input resistance of the amplifier equal to the source resistance R_S, while L_g is used to set the resonance frequency.

Assuming that $\omega^2 R^2 C^2 >> 1$, L_s can be determined as

$$L_s = \frac{R_s}{\omega_T} \cdot \frac{\left(C_{gs} + C_{gb}\right)}{C_{gs}} \quad (20)$$

where ω_T, C_{gs}, C_{gb} depend on the inversion level and on the transistor's dimensions. Accordingly L_g is given by

$$L_g = \frac{1}{\omega_0^2 \left(C_{gb} + C_{gs}\right)} \quad (21)$$

4.2. Noise Figure

The noise figure of the LNA can be calculated by analyzing the circuit shown in figure 7. The analysis based on this circuit neglects the contribution of subsequent stages to the amplifier noise figure. The use of a cascoded first stage helps to ensure that this approximation will not introduce serious errors [2].

The noise factor for an amplifier is defined as [5]

$$F \equiv \frac{Total \cdot output \cdot noise}{Total \cdot output \cdot noise \cdot due \cdot to \cdot the \cdot source} \quad (22)$$

To evaluate the output noise of the amplifier, its transconductance should be evaluated first. At the resonance frequency the squared magnitude of the transconductance is

$$\left|G_m\right|^2 = \frac{\omega_T^2}{\omega_0{}^2 R_s^2 \cdot \left[1 + \frac{\omega_T L_s}{R_s} \cdot \frac{C_{gs}}{\left(C_{gs} + C_{gb}\right)}\right]^2} \quad (23)$$

In this expression, which is valid at the resonance frequency ω_0, R_g and R_l have been neglected considering the source resistance, R_s. (23) differs from that in [2] by the term that includes C_{gb} in the denominator.

To determine the noise figure of the amplifier the procedure is the same of that presented in [2].

Using (23), the output noise power density due to the source is

$$S_{a,Rs}(\omega_0) = \frac{4KT\omega_T^2}{\omega_0^2 R_s \left(1 + \frac{\omega_T L_s}{R_s} \cdot \frac{C_{gs}}{\left(C_{gs} + C_{gb}\right)}\right)^2} \quad (24)$$

The dominant noise contributor internal to the LNA is the channel current noise of the first MOS device [2]. Recalling the expression for the power spectral density of this source (15) one can derive that the output noise power density arising from the source is

$$S_{a,id} = \frac{S_{id}}{\left(1 + \frac{\omega_T L_s}{R_s} \frac{C_{gs}}{\left(C_{gs} + C_{gb}\right)}\right)^2} \quad (25)$$

The amplitudes of the correlated portion of the gate noise and the drain noise must be summed together before the powers of the various contributors are summed. By doing so it yields a term representing the combined effect of the drain noise and the correlated portion of the induced gate noise

$$S_{a,id,ig_c}(\omega_0) = \frac{4KT \cdot \gamma \cdot \kappa \cdot g_{ms}}{\left(1 + \frac{\omega_T L_s}{R_s} \cdot \frac{C_{gs}}{\left(C_{gs} + C_{gb}\right)}\right)^2} \quad (26)$$

where

$$\kappa = \left[1 + |c| \frac{Q_L}{n} \sqrt{\frac{\delta}{5\gamma}}\right]^2, \quad (27)$$

$$\gamma = \frac{1}{\sqrt{1+i_f} + 1}\left[\frac{2}{3}\left(\sqrt{1+i_f} - 1\right) + 1\right], \quad (28)$$

and

$$Q_L = \frac{1}{\omega_0 R_s \left(C_{gs} + C_{gb}\right)}. \quad (29)$$

The last noise term is the contribution of the uncorrelated portion of the induced gate noise. Its contribution has the following power spectral density:

$$S_{a,id,ig_u}(\omega_0) = \frac{4KT \cdot \gamma \cdot \xi \cdot g_{ms}}{\left(1 + \frac{\omega_T L_s}{R_s} \cdot \frac{C_{gs}}{\left(C_{gs} + C_{gb}\right)}\right)^2} \quad (30)$$

where

$$\xi = \frac{\delta}{5\gamma} \cdot \frac{1}{n^2}\left(1 + |c|^2\right) \cdot Q_L^2 \quad (31)$$

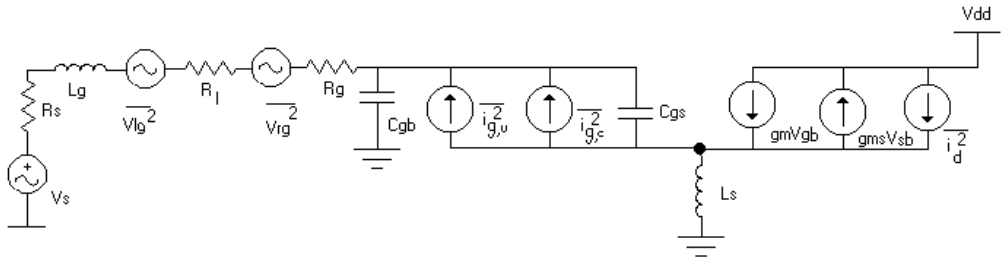

Figure7. LNA small-signal model for noise calculations

The total noise contribution of M1 is

$$S_{a,M_1}(\omega_0) = \frac{4KT \cdot \gamma \cdot \chi \cdot g_{ms}}{\left(1 + \frac{\omega_T L_s}{R_s} \cdot \frac{C_{gs}}{(C_{gs} + C_{gb})}\right)^2} \qquad (32)$$

where

$$\chi = \kappa + \xi \,. \qquad (33)$$

Using the noise figure definition together with (22) and (32), the noise figure of the LNA is

$$F = 1 + g_{ms} \cdot \gamma \cdot \chi \cdot \left(\frac{\omega_0^2}{\omega_T^2}\right). \qquad (34)$$

All the terms of (34) are functions of the inversion level. figure 8 shows the noise figure of the amplifier for several inversion levels, in the moderate inversion region, as the W/L of the input transistor varies. It can be noticed that there is a minimum for each curve, and as expected the noise figure decreases as the inversion level increases.

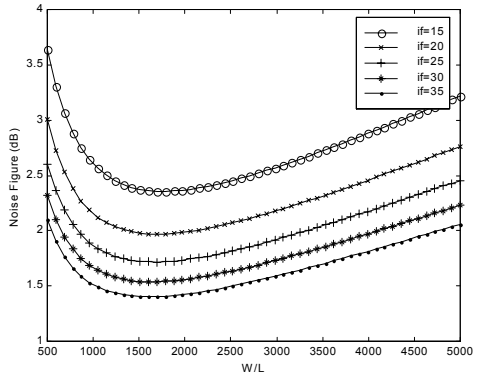

Figure 8. Noise figure versus W/L for several inversion levels for a frequency of 2.5 GHz

5. LNA DESIGN EXAMPLE

In this section an example is used to show a design methodology based on the equations developed in the previous sections. Table 1 summarizes the design parameters

The first step in our procedure is the choice of the inversion level. Although the inversion level should be as low as possible, the resonance frequency should not be close of the intrinsic cutoff frequency. So the inversion level is chosen such that the ratio ω_T/ω_0 is larger than five. With the aid of (11) and figure 9 the inversion level is chosen to be 35.

Next, for the parameters in table 1 and the specified i_f , L_s is determined from (20). There should be a tradeoff between the value of L_g and the noise figure of the amplifier because both depend on the width of M_1. The width is determined, with the aid of figure 8, to minimize the noise figure.

Table 1. LNA design parameters

Symbol	Quantity	Values
L	Length	0.35 µm
f_0	Resonance frequency	2.5 GHz
R_S	Source resistancer	50 Ω
V_{DD}	Suply voltage	2.5 V

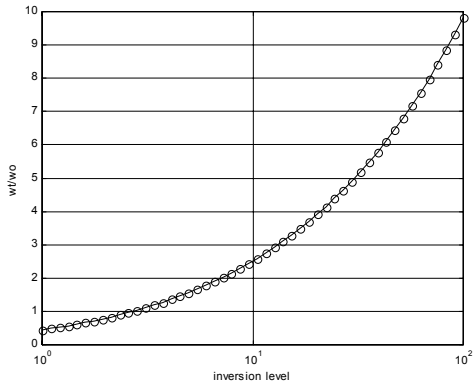

Figure 9. Relationship between ω_T/ω_0 versus i_f for $\omega_0 = 2.\pi.2{,}5.10^9$ rad/s

Finally the value of L_g is calculated from (21). If L_g results too large to be integrated then W or the inversion level could be increased. The value of L_d is chosen to adjust the gain and the output resonance frequency and is dependent on the load at the output node. In this example L_d is external to the chip. For simplicity, the dimensions of M_2 are the same as M_1. The results are summarized in Table 2.

Table 2. LNA design results

Symbol	Quantity	Values
W	width	525 μm
L_g	gate inductor	7,6 nH
L_s	source inductor	0,7 nH
NF	noise figure	1,4 dB
I_d	drain current	4,1 mA

6. SIMULATION RESULTS

The amplifier was simulated in SMASH circuit simulator using the ACM model, and the parameters for a TSMC 0.35 μm CMOS process.

Figure 10 shows that the accuracy of the model used for the magnitude of the input impedance of the LNA is very good in comparison with the simulation results. Differences of less than 10% were obtained in the magnitude of the input impedance and in the resonance frequency.

As the simulation model does not include the induced gate noise the simulation can only be used to evaluate the noise figure due to thermal noise. Figure 11 shows that the simulated noise figure agrees well to the calculated one just considering the thermal noise in the channel. Figure 11 also shows that the induced gate noise must be included in simulation models for a good evaluation of the noise figure before fabrication.

7. CONCLUSION

We presented a design methodology for RF CMOS LNAs using a current-based MOSFET model. The main advantage of this methodology is that it is valid in all regions of operation of the MOS transistors.

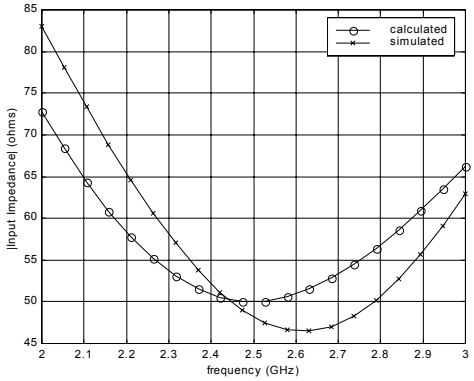

Figure10. Magnitude of the input impedance of the LNA, calculated using (19a) and simulated in SMASH using the ACM model.

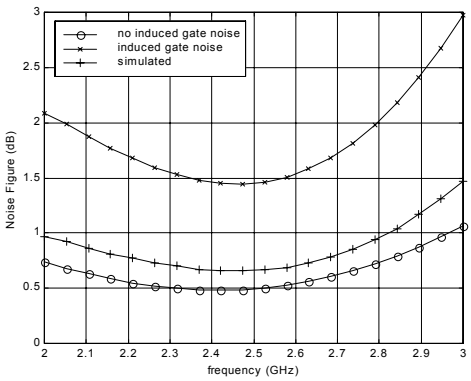

Figure11. Noise figure versus frequency.

It was shown that it is possible to move the operating point of RF devices from strong inversion to moderate inversion taking advantage of higher g_m/I_D ratio, without degrading the noise figure. Although the transistors that operates in moderate inversion are larger than those in strong inversion, the increase in area is not significant as the integrated inductors are much bigger.

An LNA was designed to illustrate the methodology, and the simulation results showed the feasibility of this approach as a design method.

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