

# **CAPÍTULO 3**

## **INVERSOR CMOS**

Baseado nos slides de Peter Cheung  
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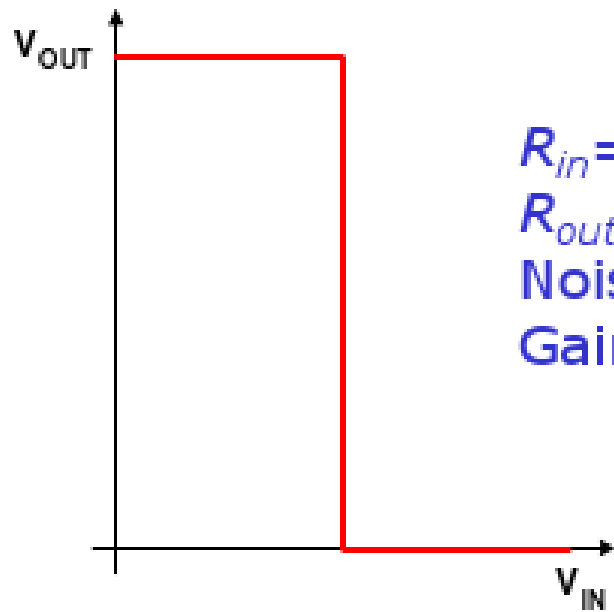
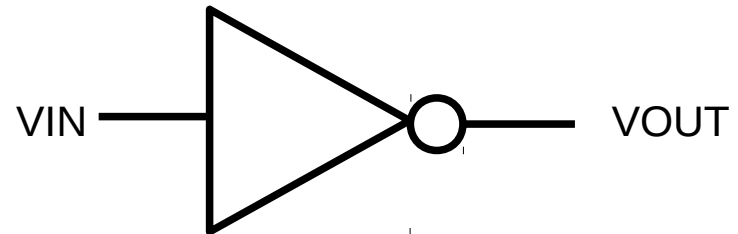
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# OBJETIVOS

1. Compreender o funcionamento do inversor CMOS
2. Identificar os parâmetros fundamentais do inversor CMOS
3. Analisar e dimensionar inversores CMOS
4. Simulação elétrica e caracterização de inversores

# INVERSOR IDEAL



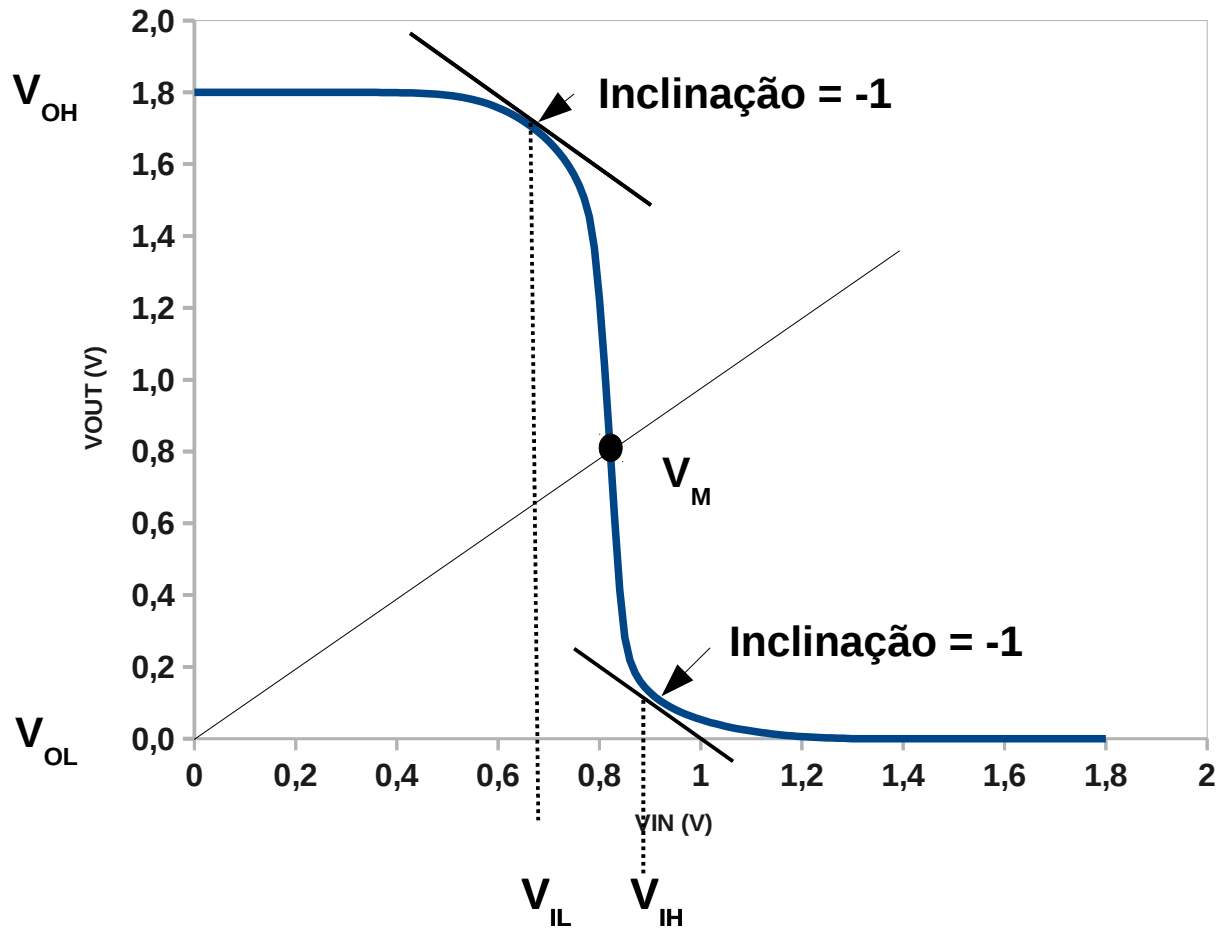
$$R_{in} = \infty$$

$$R_{out} = 0$$

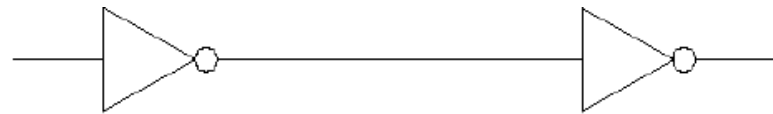
$$\text{Noise Margin} = V_{DD}/2$$

$$\text{Gain} = \infty$$

# NÍVEIS LÓGICOS

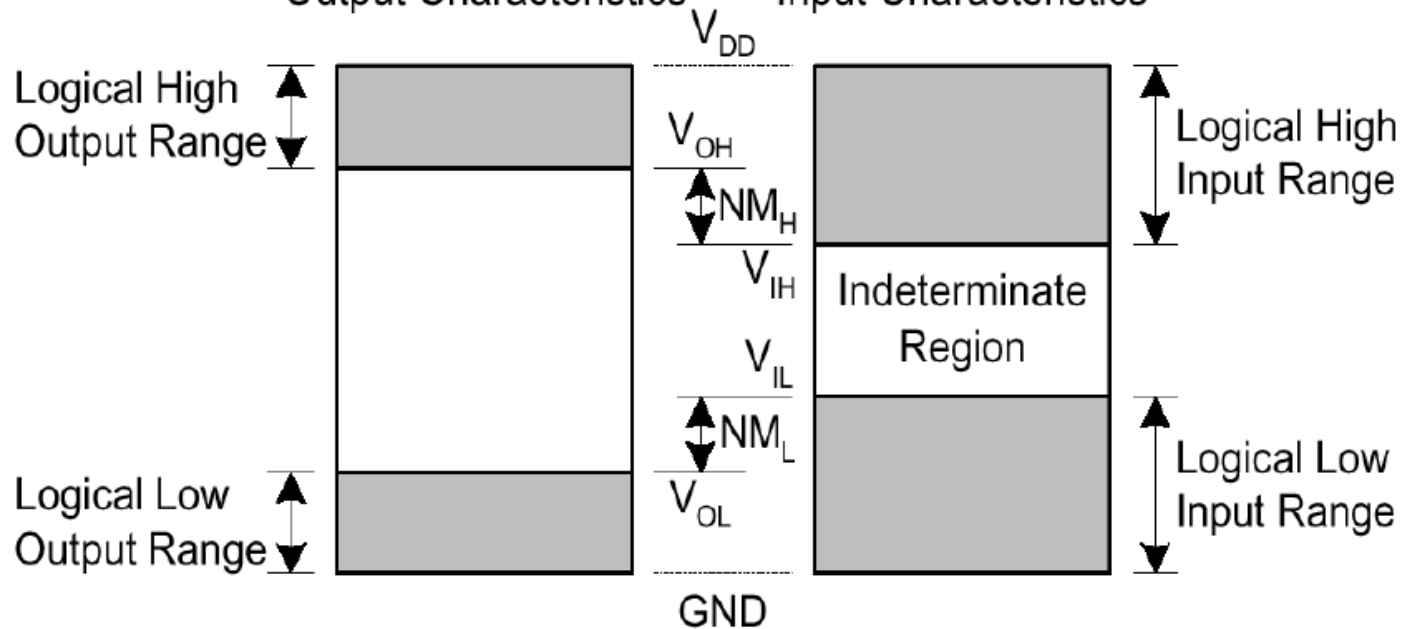


# MARGENS DE RUÍDO



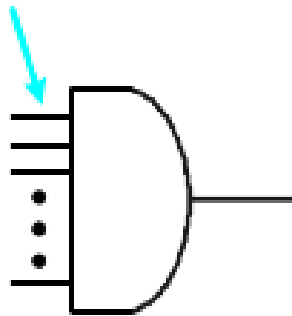
Output Characteristics

Input Characteristics



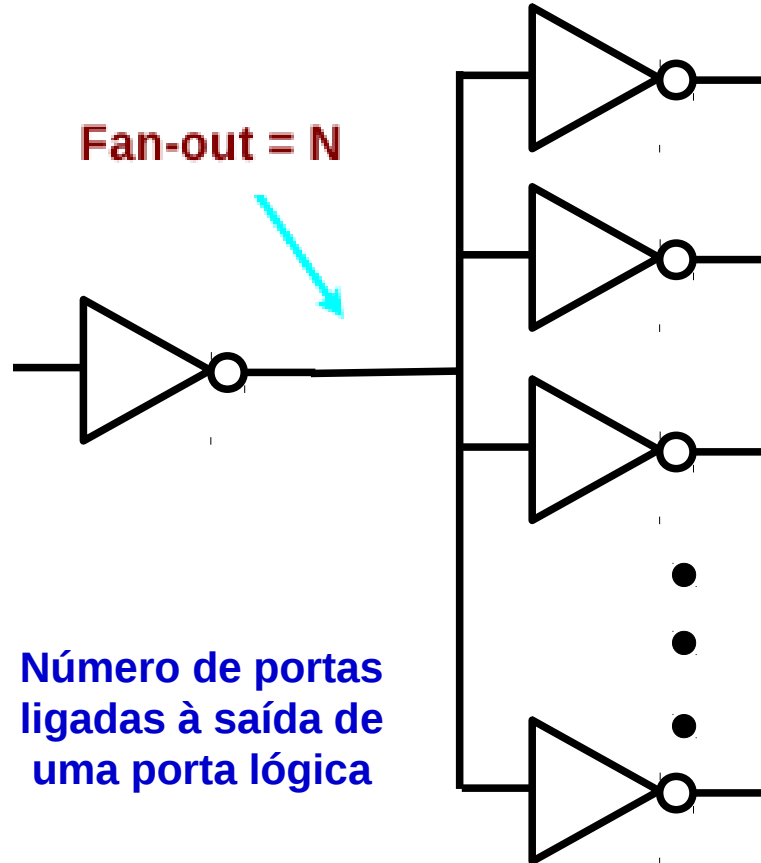
## Fan-In e Fan-Out

Fan-in = M



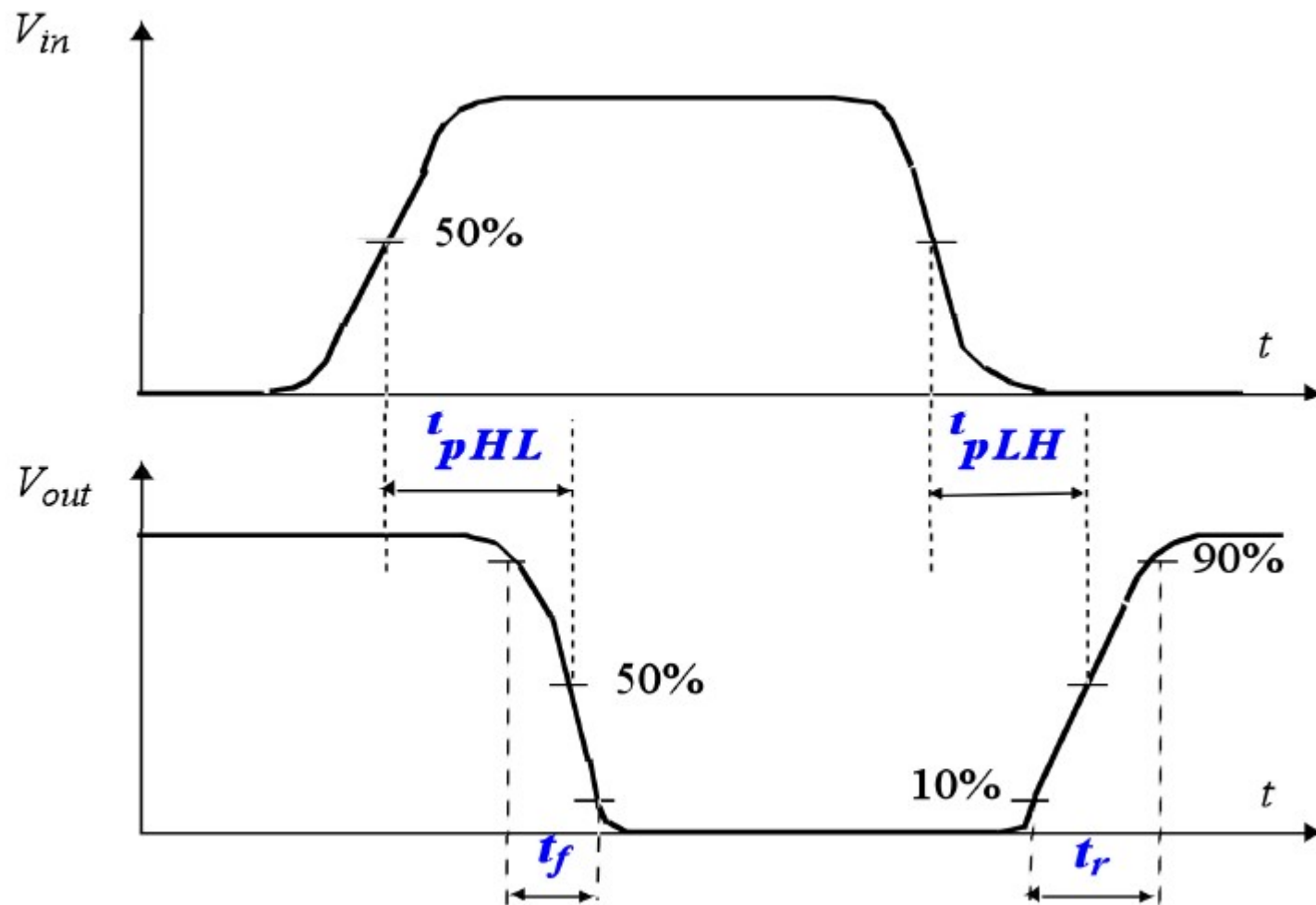
Número de entradas ligadas a uma porta lógica

Fan-out = N

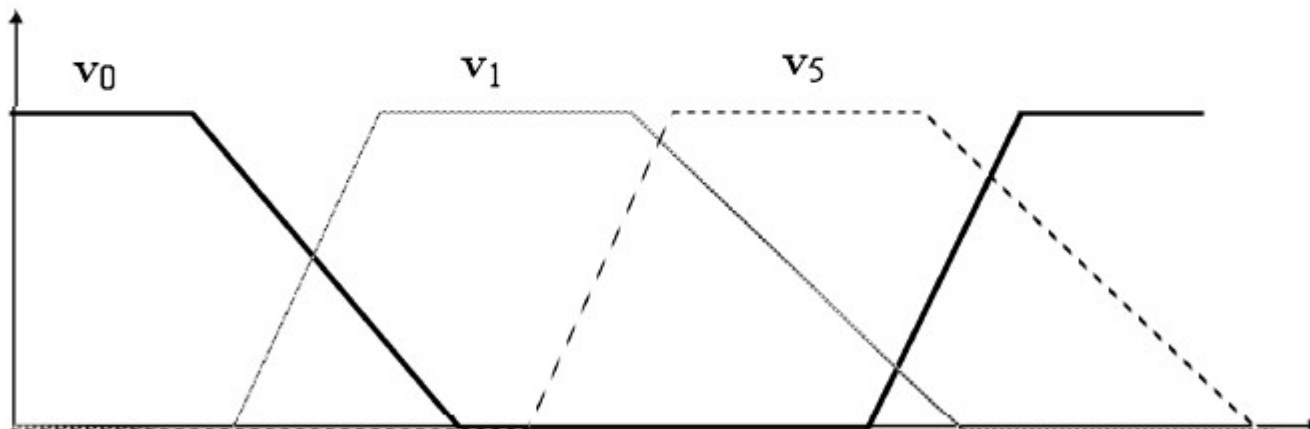
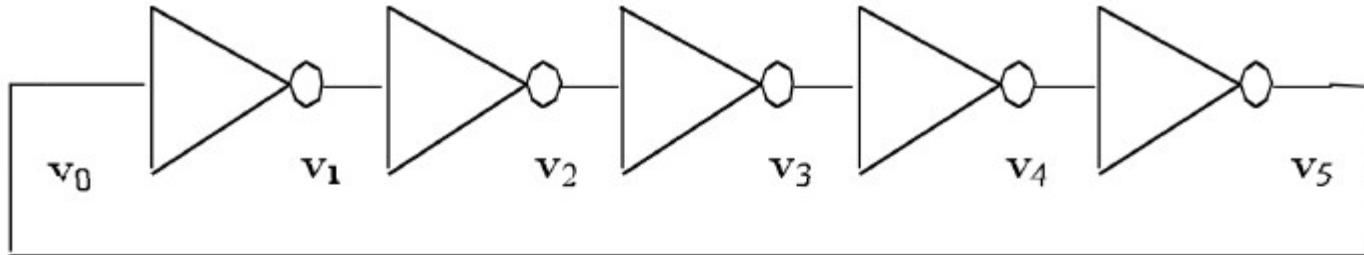


Número de portas ligadas à saída de uma porta lógica

# COMPORTAMENTO DINÂMICO



## OSCILADOR EM ANEL



$$T = 2 \times t_p \times N$$



# DISSIPACÃO DE POTÊNCIA

**Potência máxima**  $P_{max} = V_{DD} * I_{DD}$

**Potência média**  $P_{med} = \frac{1}{T} \int_0^T p(t) dt = \frac{V_{DD}}{T} \int_0^T i_{DD}(t) dt$

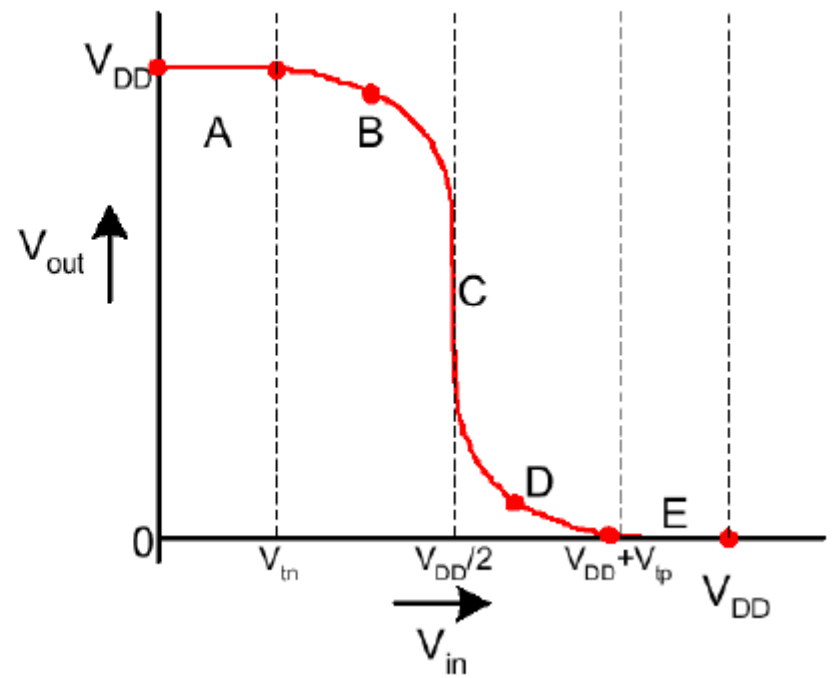
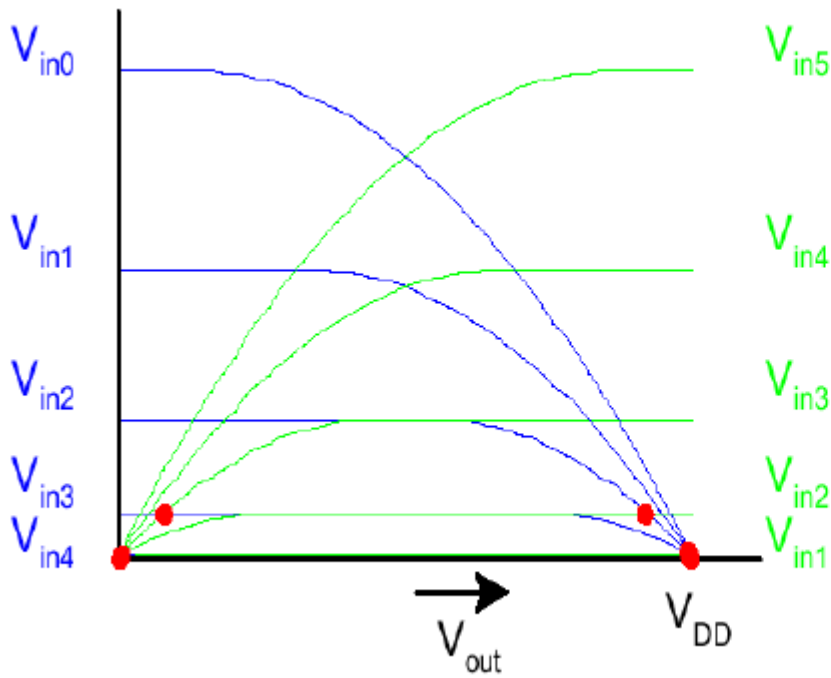
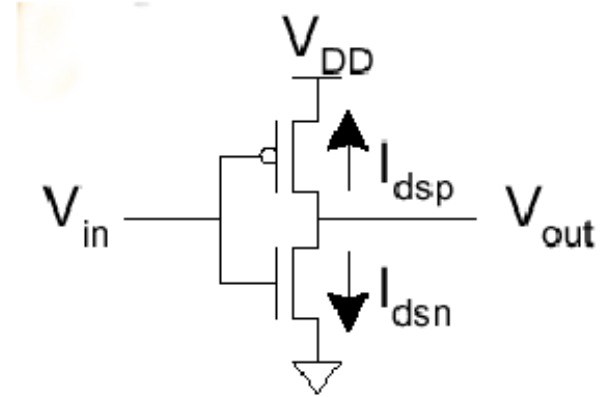
## **Produto Potência-Atraso (Power-Delay Product)**

- energia por operação de chaveamento

$$PDP = P_{med} * t_p$$

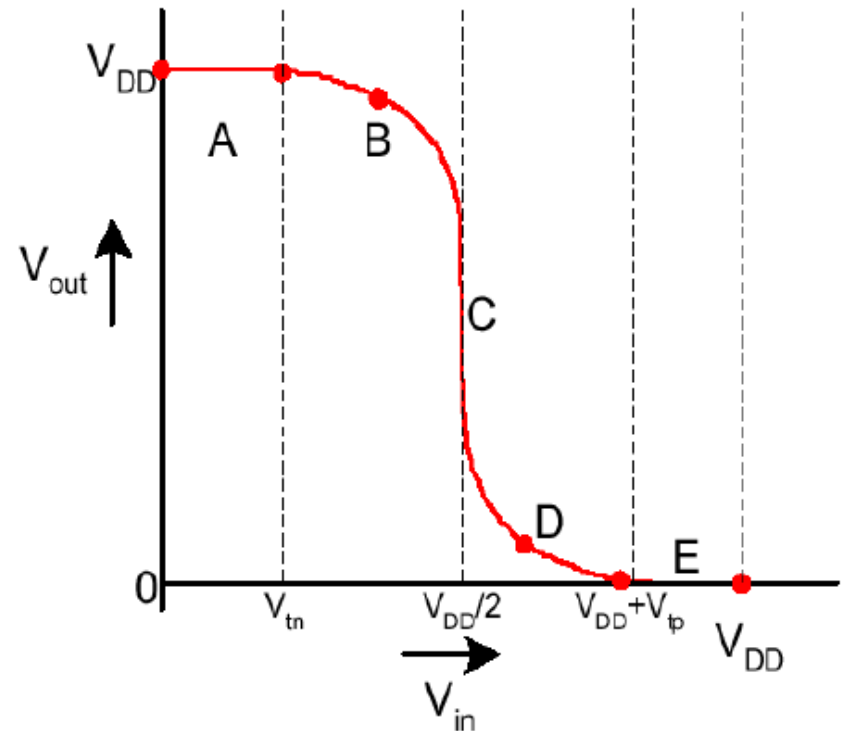
# ANÁLISE DO INVERSOR CMOS

## CARACTERÍSTICA DE TRANSFERÊNCIA DC



# REGIÕES DE OPERAÇÃO

Region	nMOS	pMOS
A	Cutoff	Linear
B	Saturation	Linear
C	Saturation	Saturation
D	Linear	Saturation
E	Linear	Cutoff



# Determinação de $V_M$

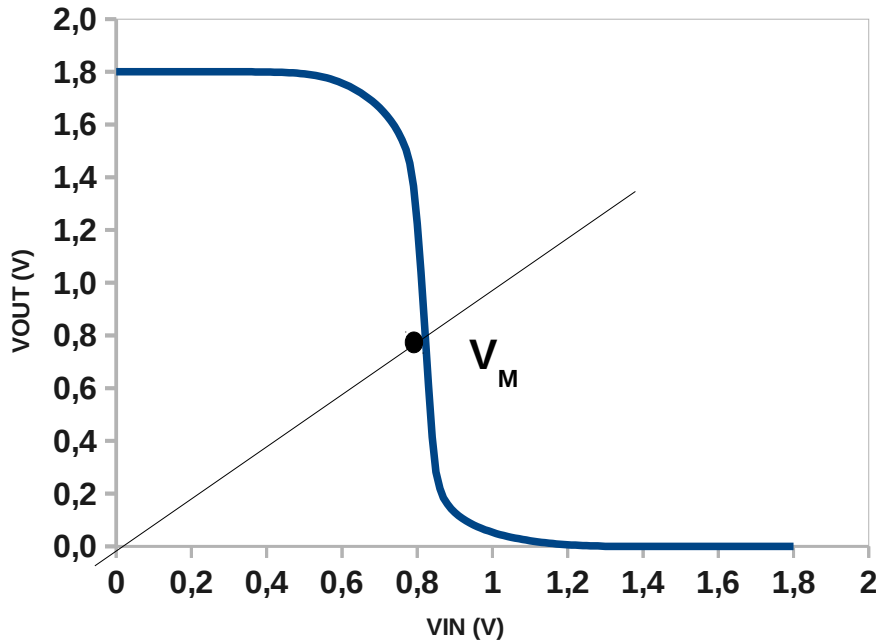
Ambos transistores saturados

$$\frac{k_n}{2}(V_M - V_{tn})^2 = \frac{k_p}{2}(V_{DD} - V_M - |V_{tp}|)^2$$

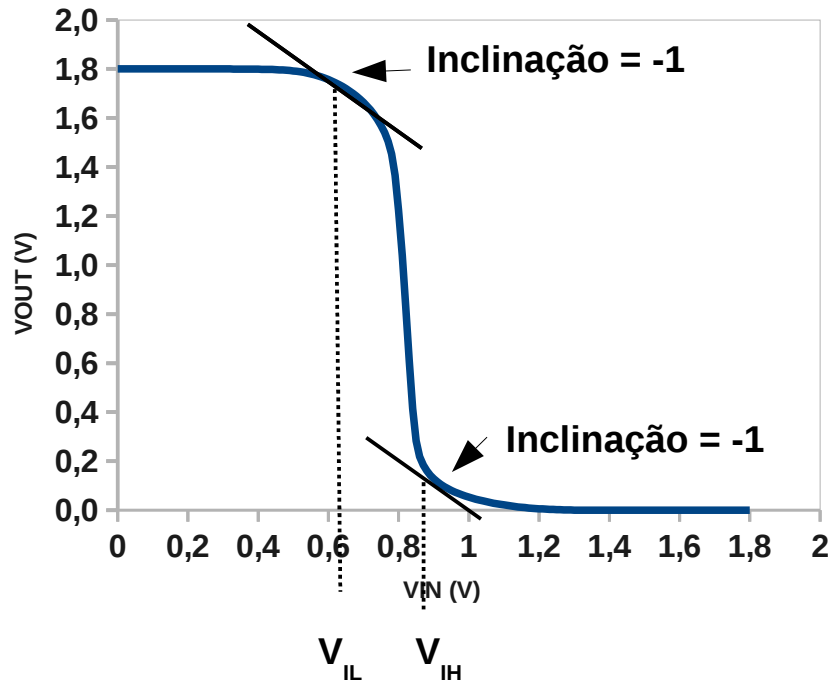
$$V_M = \frac{r(V_{DD} - |V_{tp}|) + V_t}{1 + r}$$

onde  $r = \sqrt{\frac{k_p}{k_n}}$

$$k_{n(p)} = k'_{n(p)} \left( \frac{W}{L} \right)_{n(p)}$$



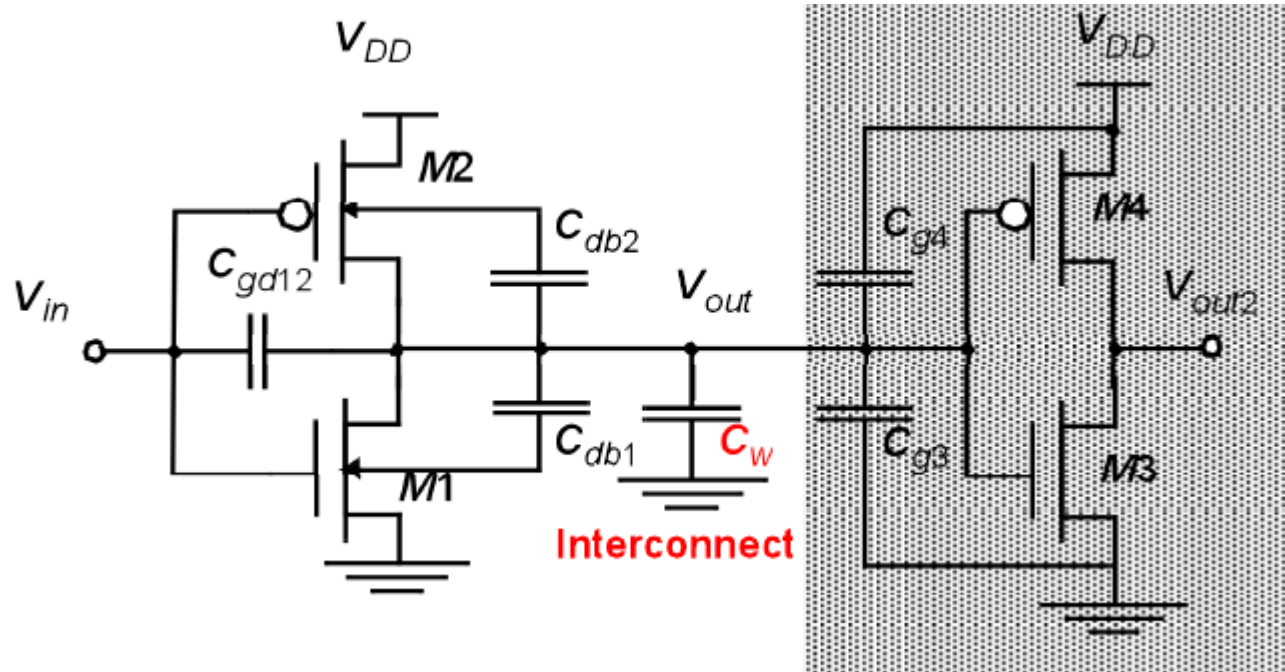
## Determinação de $V_{IL}$ e $V_{IH}$



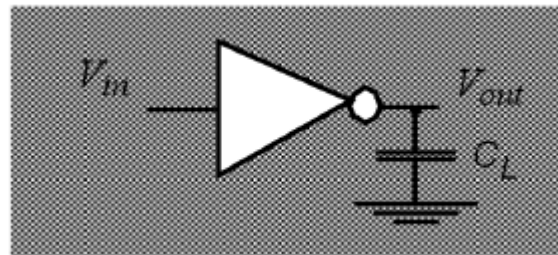
Calcular o ganho do inversor e igualar à unidade. Observar as regiões de operação dos transistores.

$$\frac{dV_{OUT}}{dV_I} = -1$$

# ANÁLISE DINÂMICA



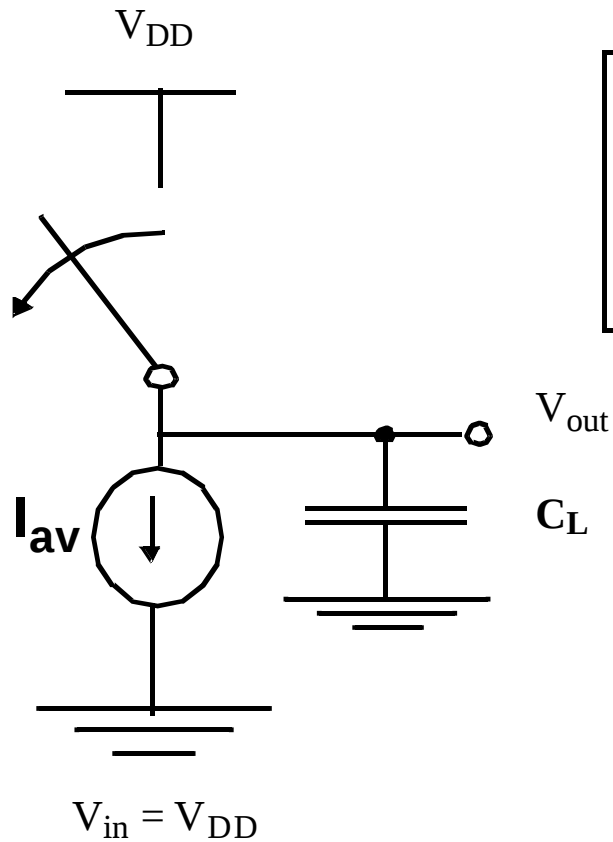
Modelo simplificado



# CÁLCULO DAS CAPACITÂNCIAS

Capacitor	Expression
$C_{gd1}$	$2 \text{ CGD0 } W_n$
$C_{gd2}$	$2 \text{ CGD0 } W_p$
$C_{db1}$	$K_{eqn} (AD_n \text{ CJ} + PD_n \text{ CJSW})$
$C_{db2}$	$K_{eqp} (AD_p \text{ CJ} + PD_p \text{ CJSW})$
$C_{g3}$	$C_{ox} W_n L_n$
$C_{g4}$	$C_{ox} W_p L_p$
$C_w$	From Extraction
$C_L$	$\Sigma$

# ATRASO DE PROPAGAÇÃO



$$t_{pHL} = \frac{C_L V_{swing}/2}{I_{av}}$$

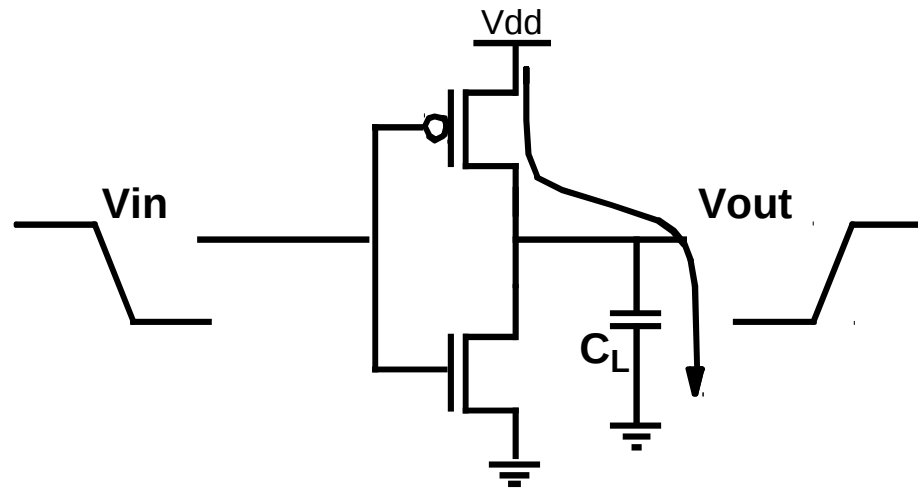
$$\sim \frac{C_L}{k_n V_{DD}}$$

Do mesmo modo para  $t_{pLH}$

$$t_{pLH} = \frac{C_L}{K_p V_{DD}}$$



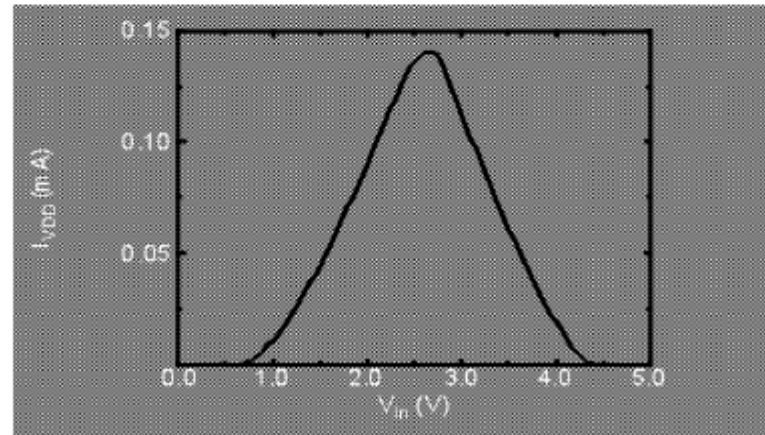
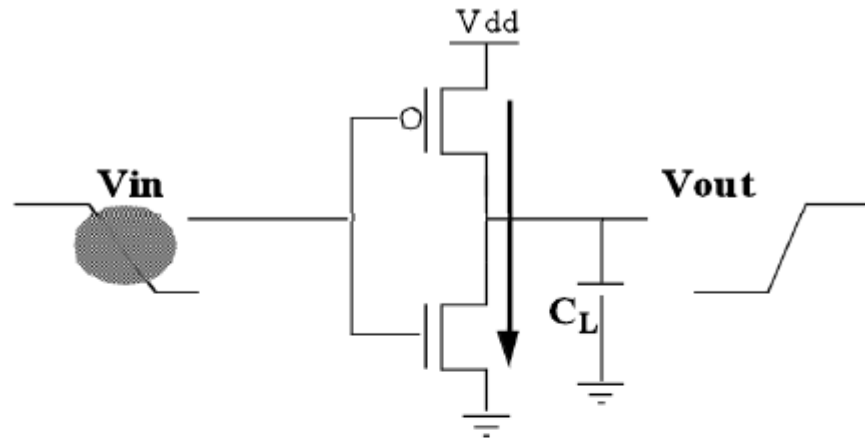
# DISSIPAÇÃO DE POTÊNCIA



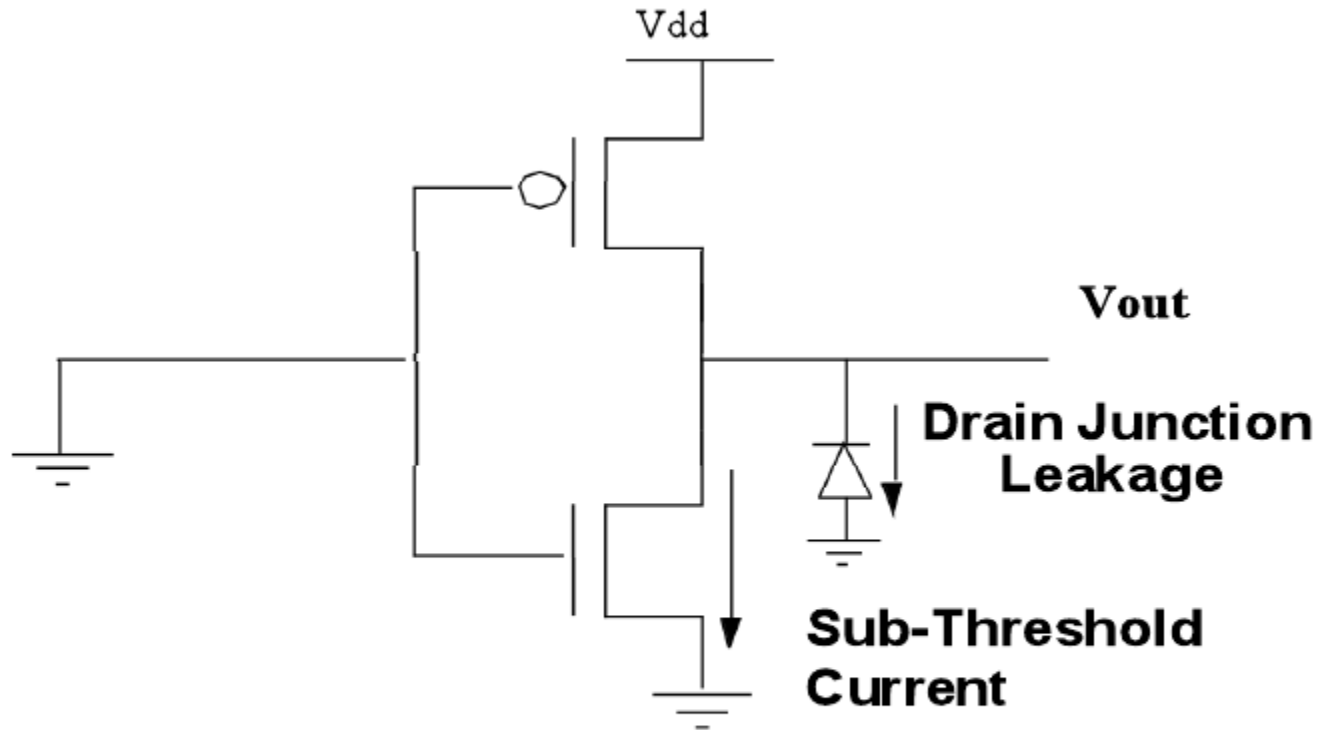
$$\text{Energy/transition} = C_L * V_{dd}^2$$

$$\text{Power} = \text{Energy/transition} * f = C_L * V_{dd}^2 * f$$

# CORRENTE DE CURTO-CIRCUITO



# CORRENTE DE FUGA



**Sub-Threshold Current Dominant Factor**