CAPÍTULO 5
CIRCUITOS LÓGICOS SEQUENCIAIS

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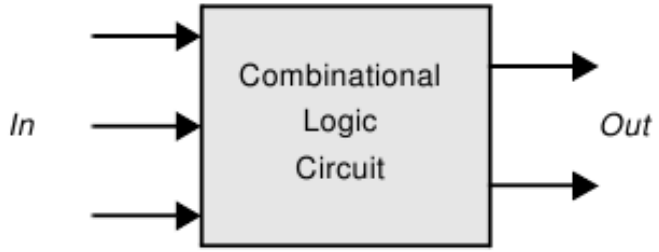
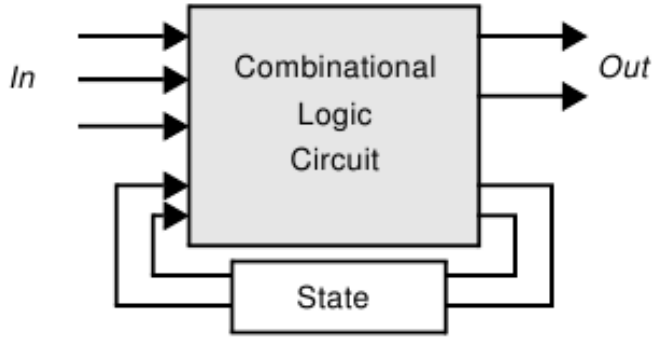
CIRCUITOS LÓGICOS COMBINACIONAIS E SEQUENCIAIS



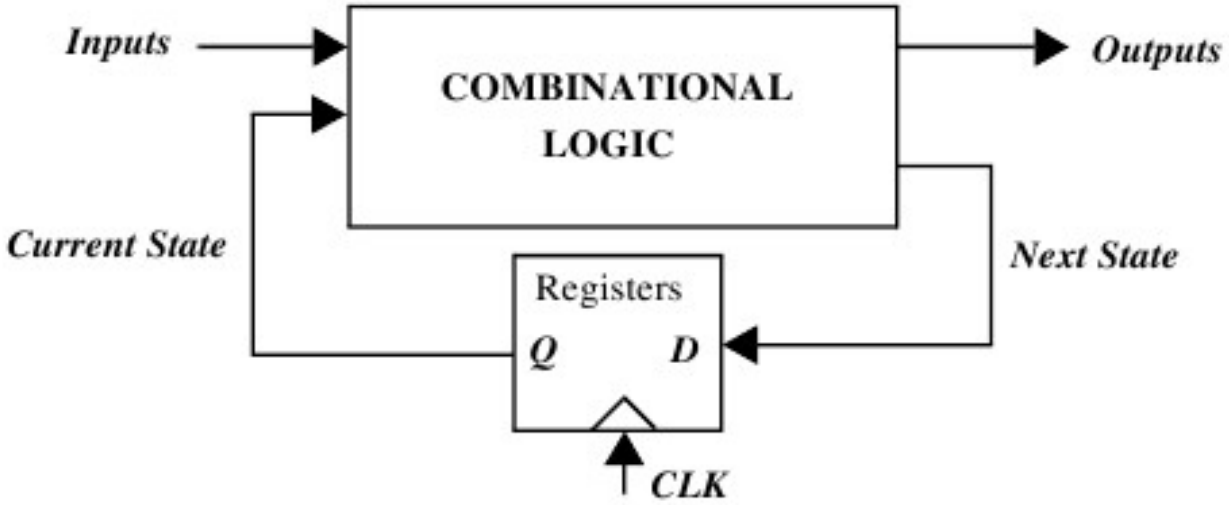
(a) Combinational



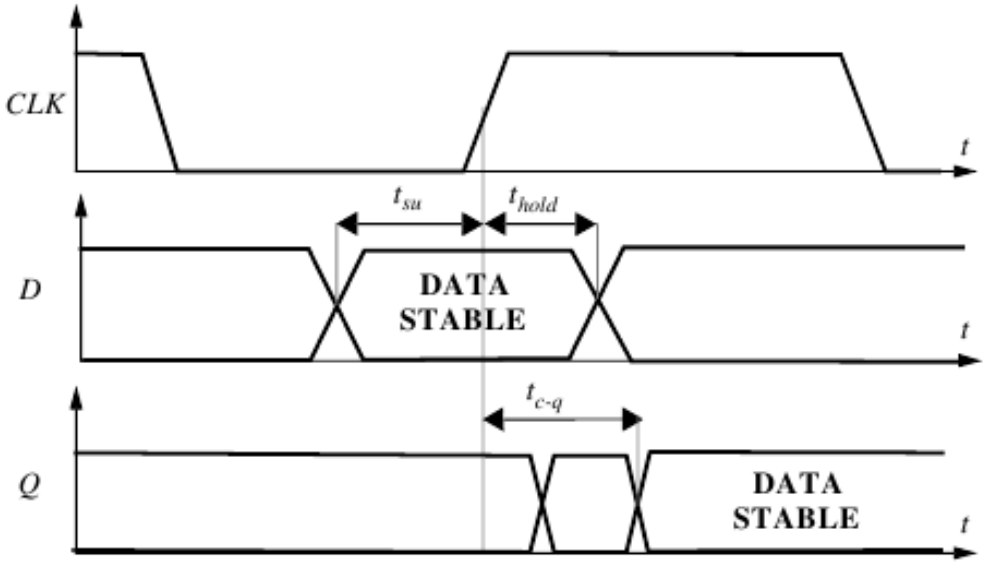
(b) Sequential

Exemplo de Circuito Sequencial

Máquina de Estados



Temporização para circuitos sequenciais



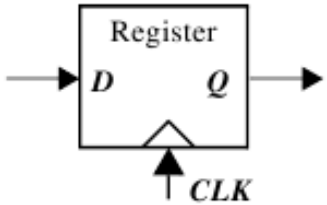
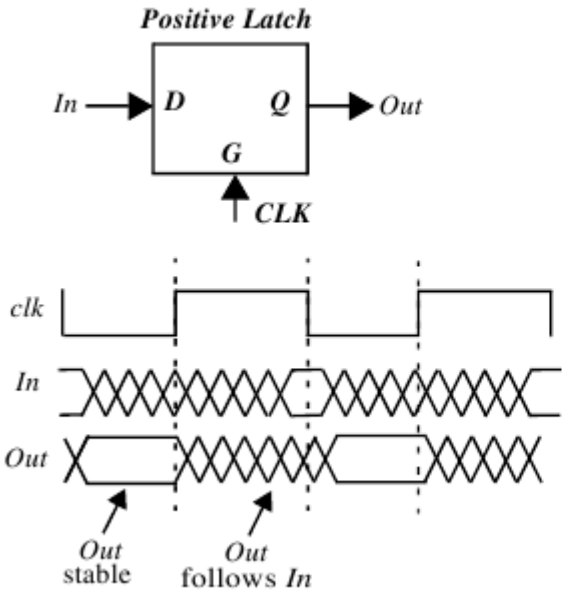
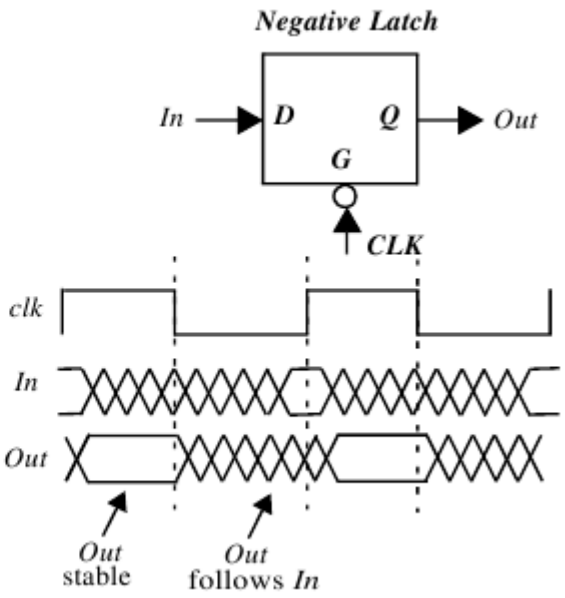


Figure 7.2 Definition of *set-up time*, *hold time*, and *propagation delay* of a synchronous register.

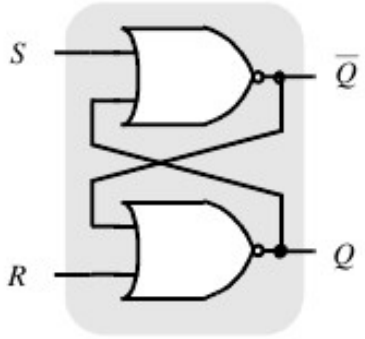
Mínimo período de Clock $T \geq t_{c\text{-}q} + t_{plogic} + t_{su}$

Latches

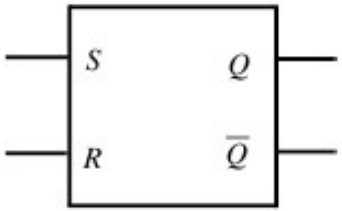

Positive Latch
In
D
Q
Out
G
CLK
clk
In
Out
Out
stable
Out
follows In


Negative Latch
In
D
Q
Out
G
CLK
clk
In
Out
Out
stable
Out
follows In

Flip-Flop SR



(a) Schematic diagram



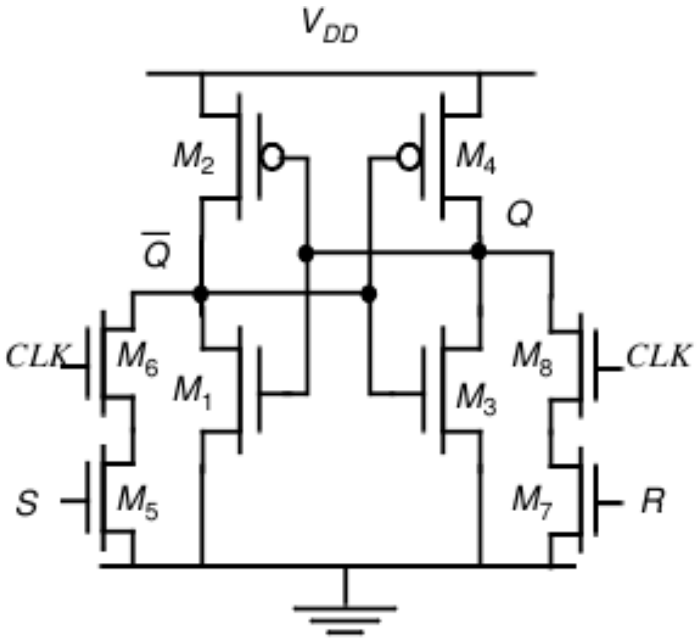
(b) Logic symbol

S	R	Q	$\overline{Q}$
0	0	Q	$\overline{Q}$
1	0	1	0
0	1	0	1
1	1	0	0

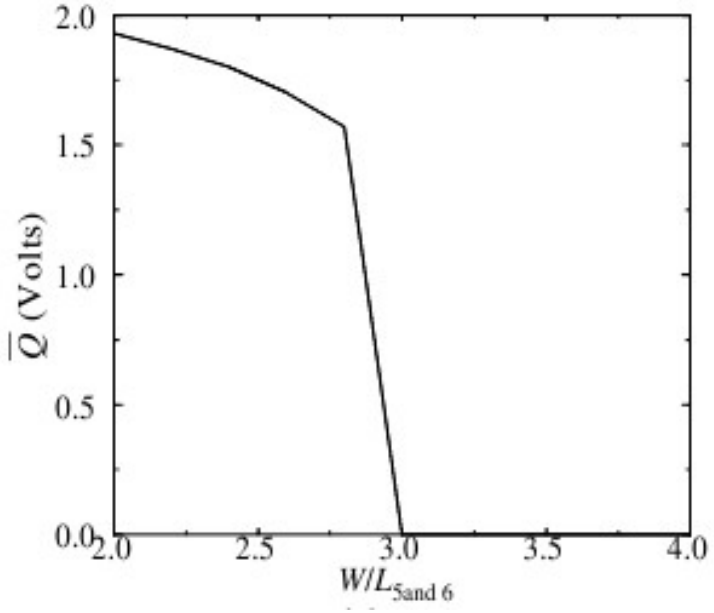
Forbidden State

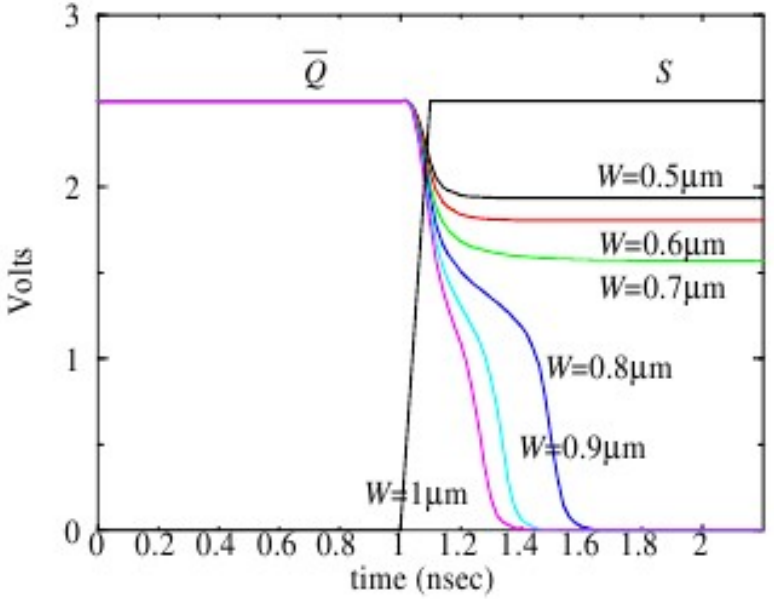
(c) Characteristic table

Flip-Flop SR CMOS com clock

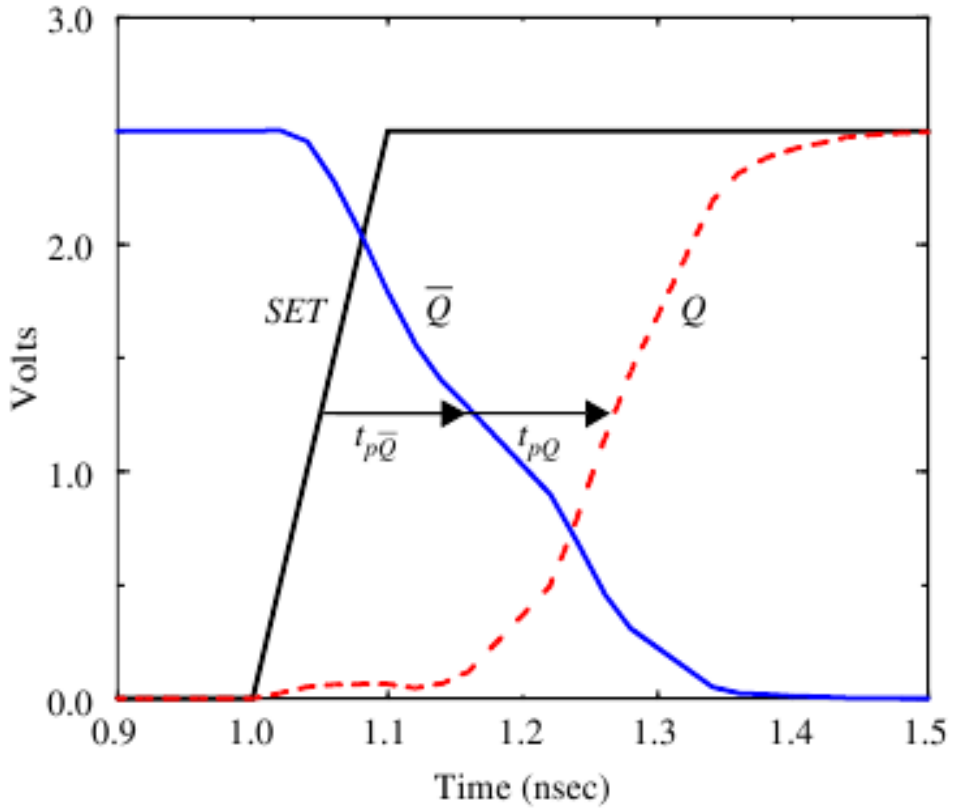


Dimensionamento



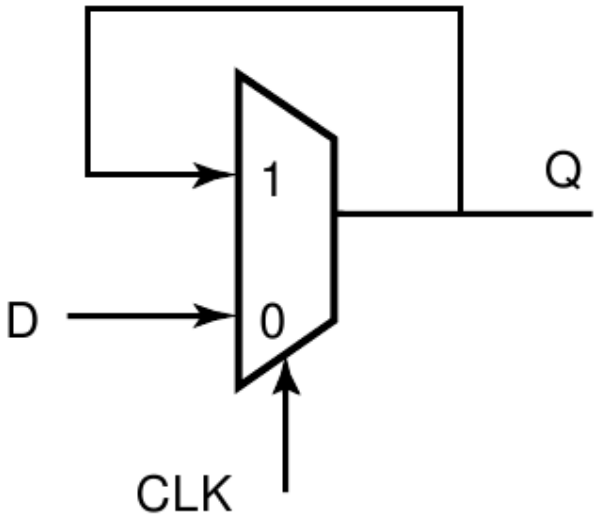


Atraso de propagação



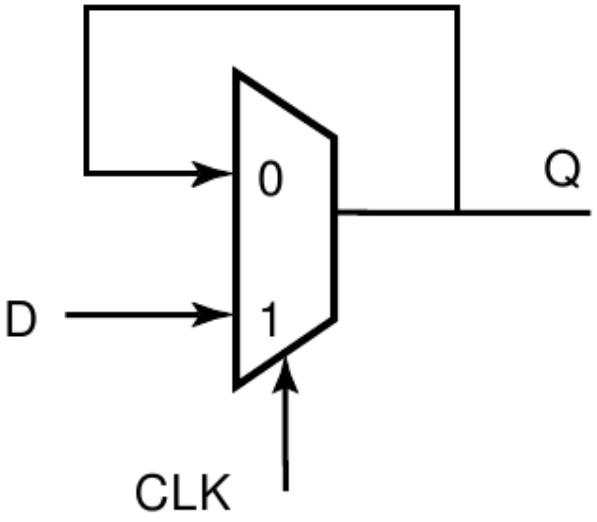
Latches baseados em multiplexadores (flip-flop tipo D)

Latch negativo



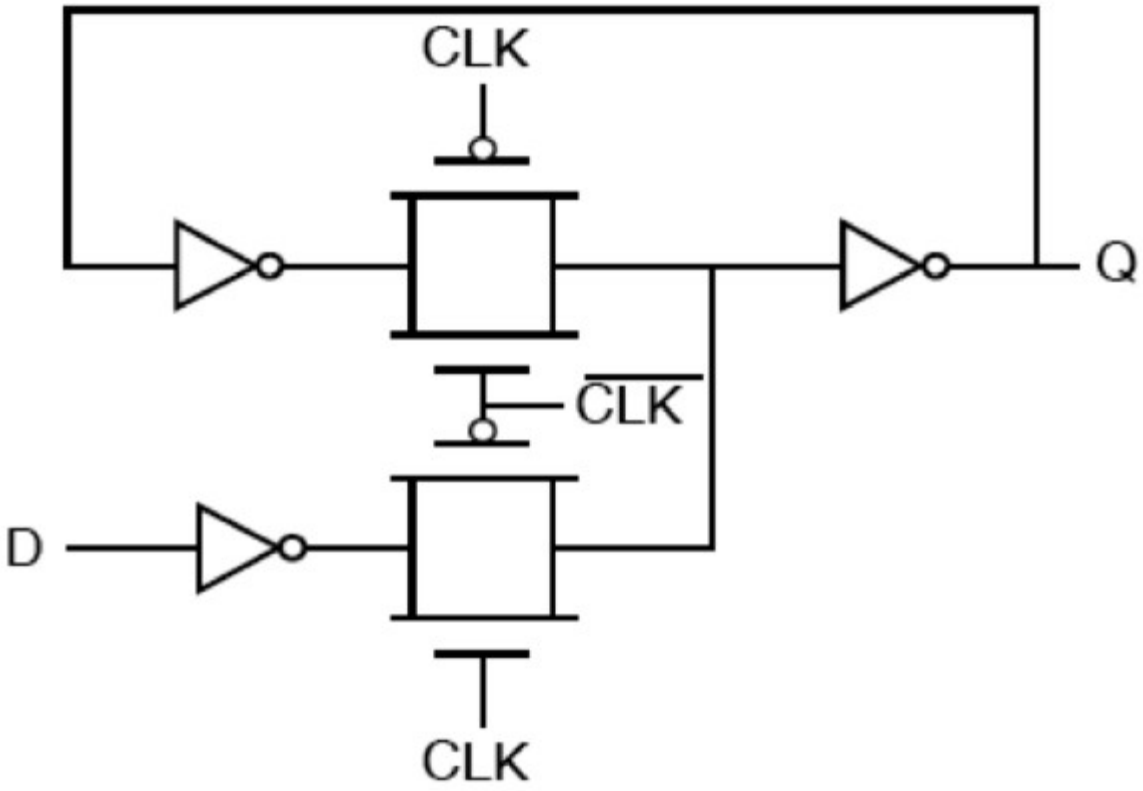
$$Q = \overline{Clk} \cdot Q + Clk \cdot In$$

Latch positivo

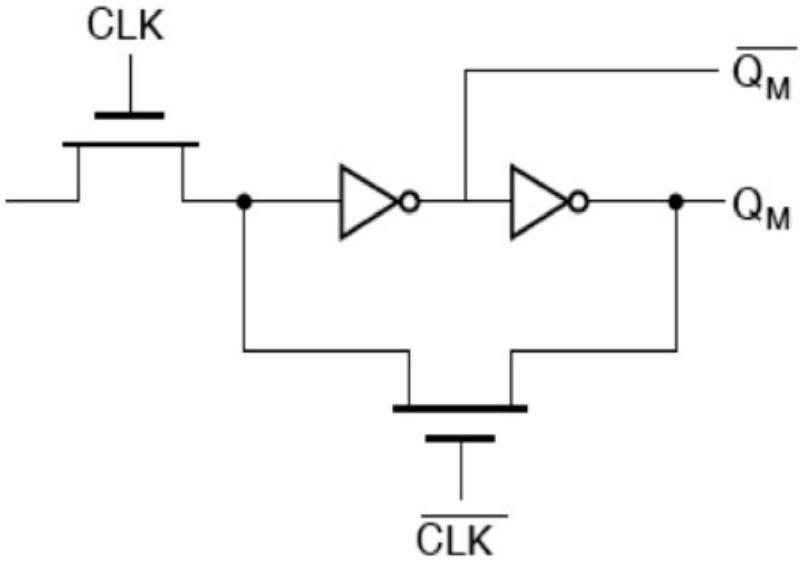


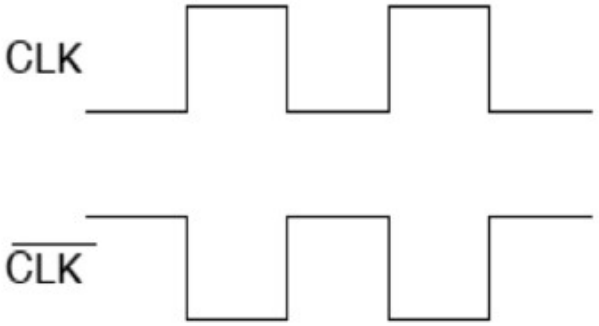
$$Q = Clk \cdot Q + \overline{Clk} \cdot In$$

Implementação com portas de transmissão

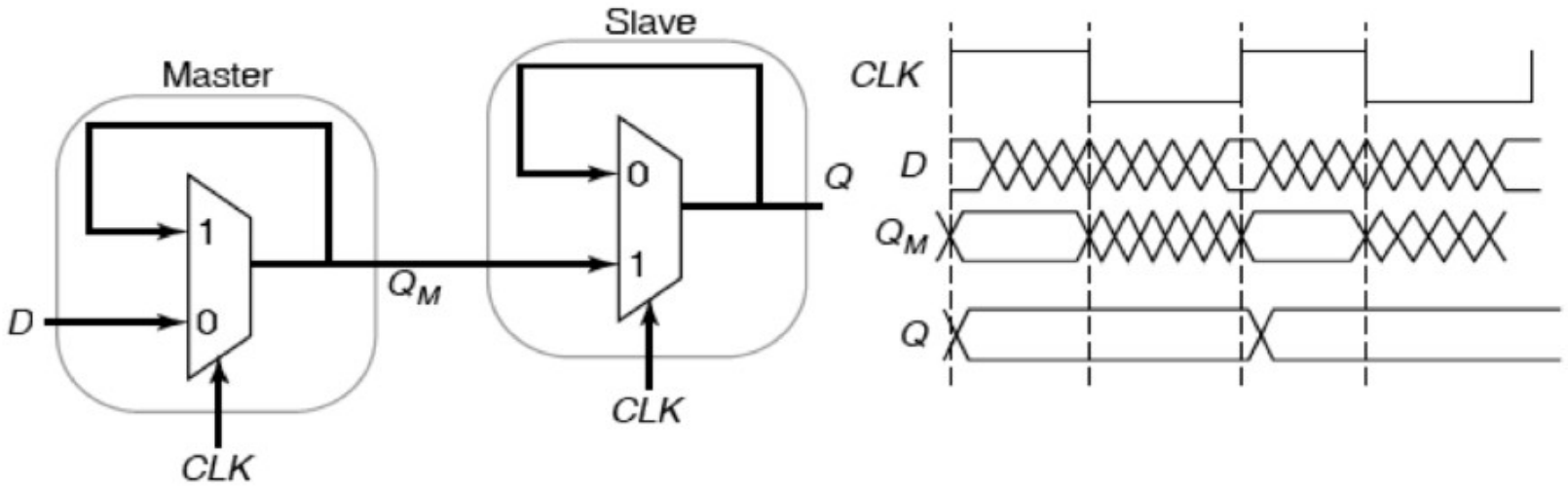


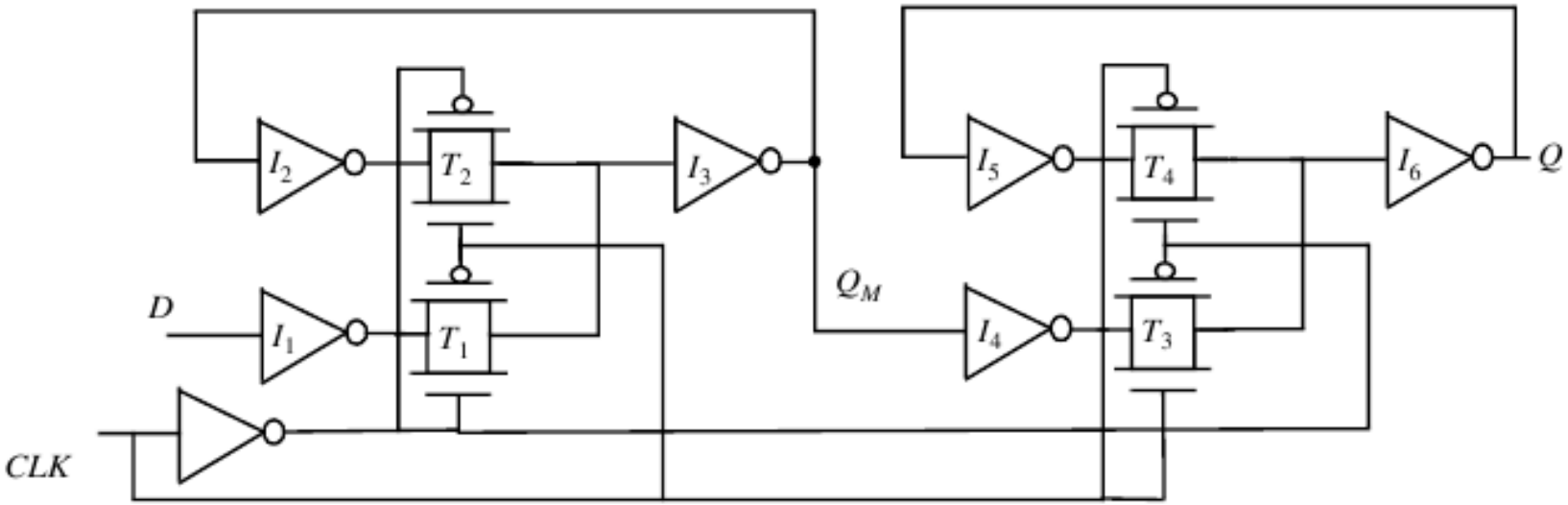
Implementação usando apenas NMOS



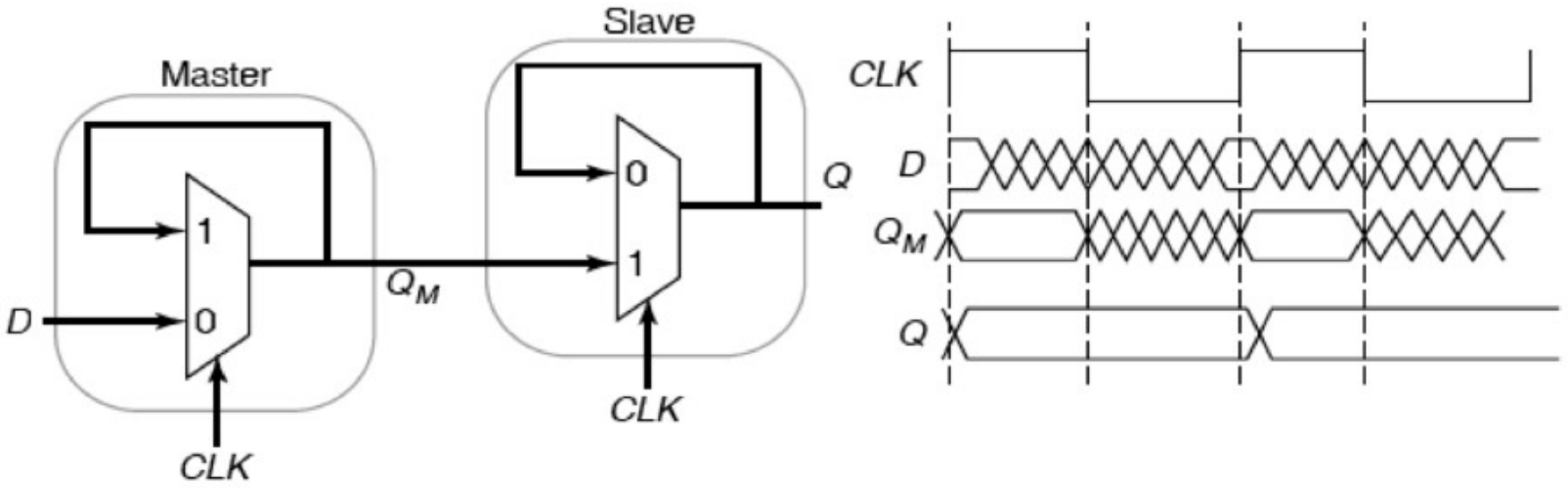


Flip-Flop D Mestre-Escravo

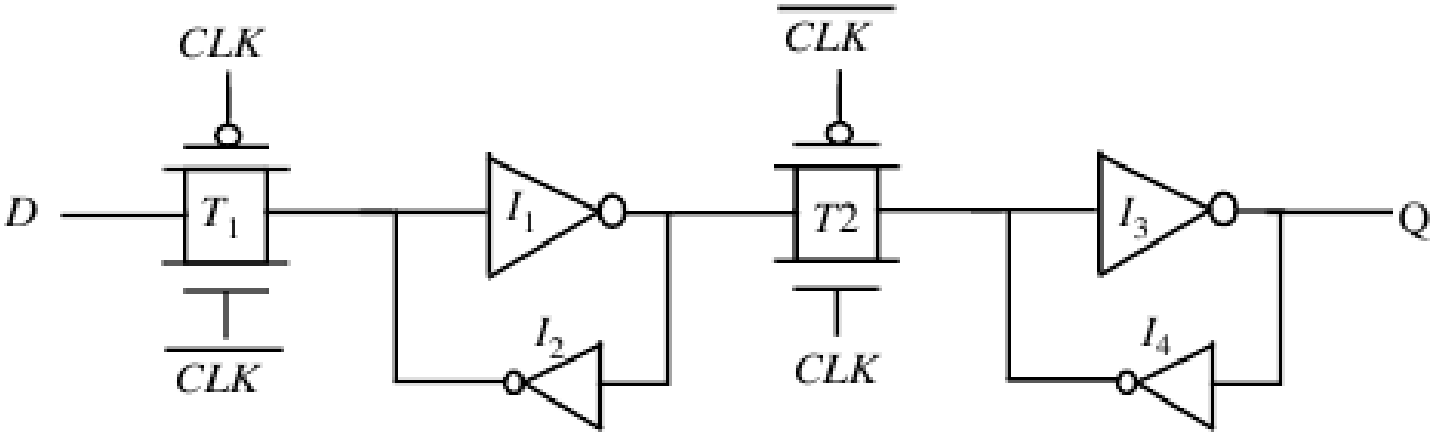



I_2
T_2
I_3
I_5
T_4
I_6
Q
Q_M
D
I_1
T_1
I_4
T_3
CLK

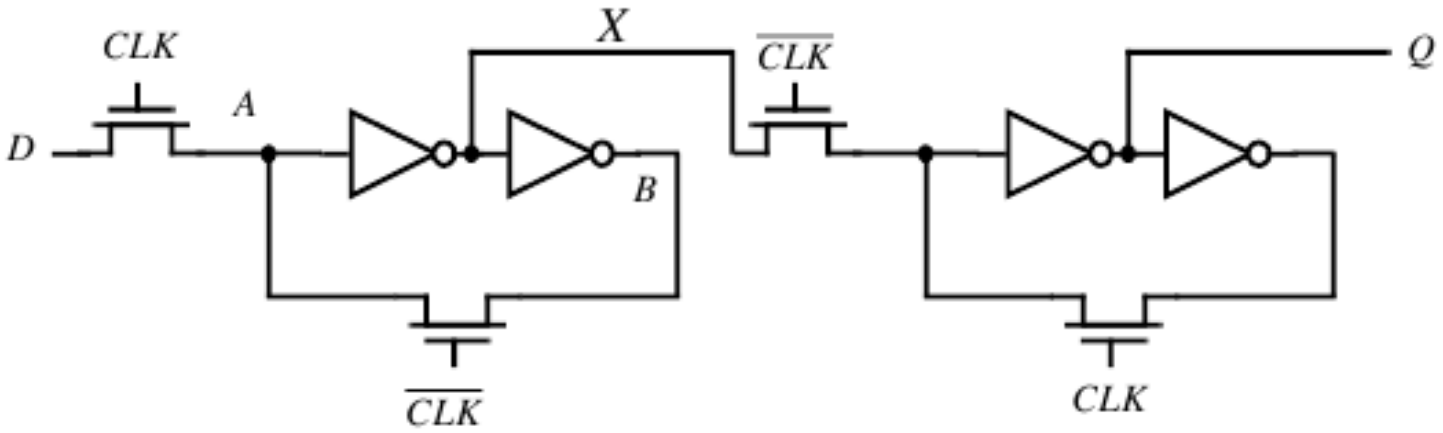
Implementação

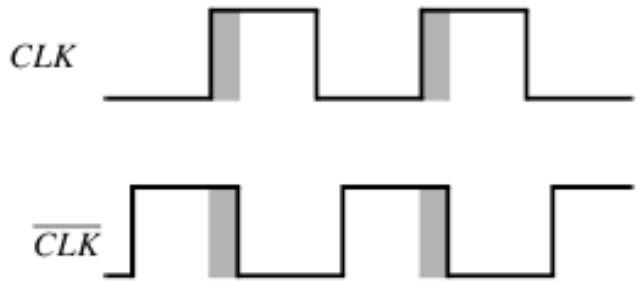


Reduzindo a carga sobre o clock

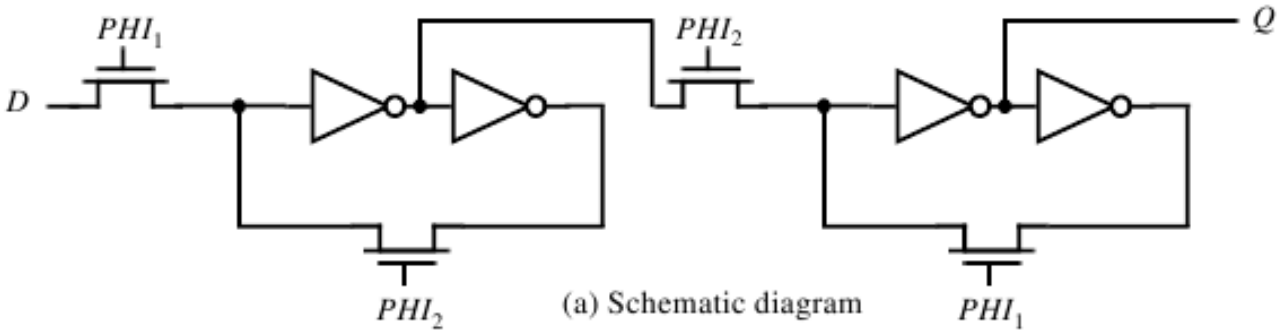


Clock não ideal

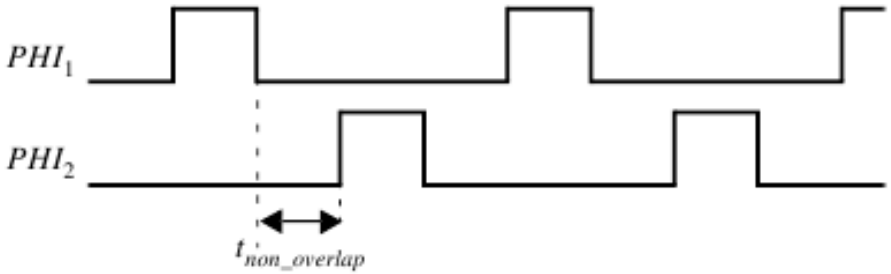




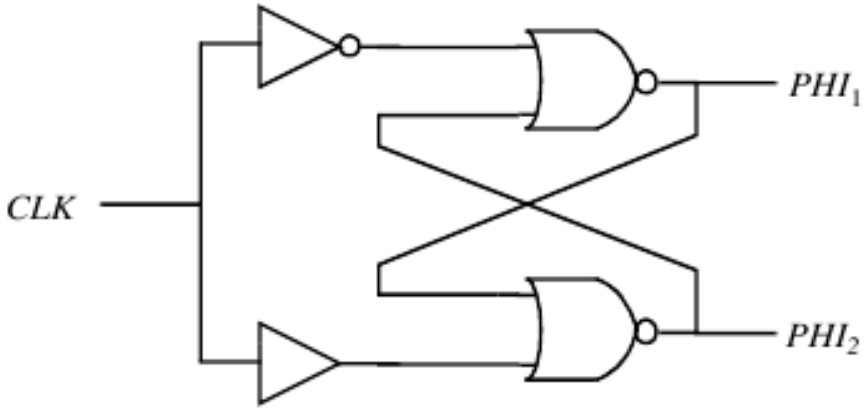
Clocks não sobrepostos



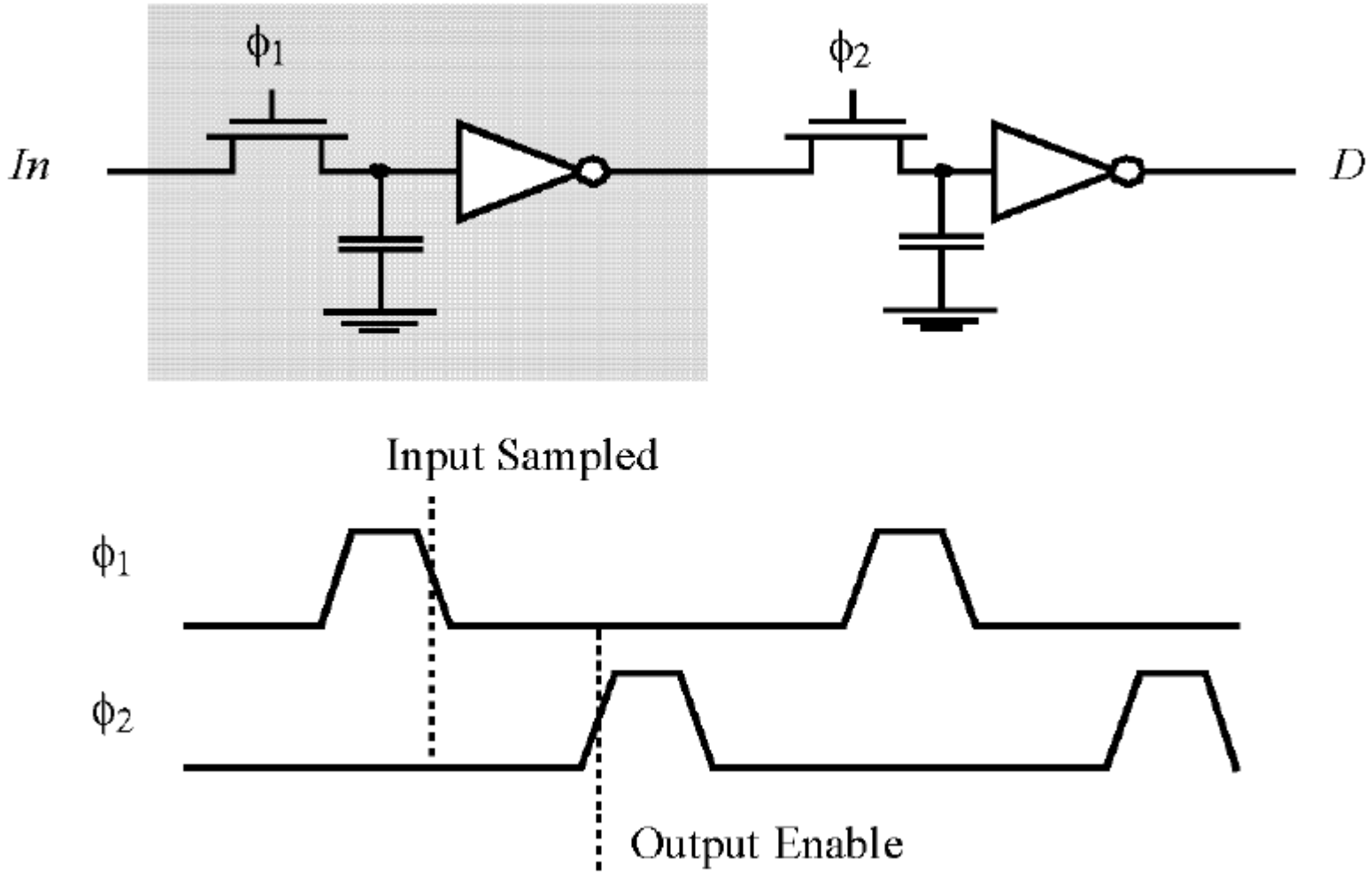
(a) Schematic diagram



Geração de duas fases de Clock não sobrepostas

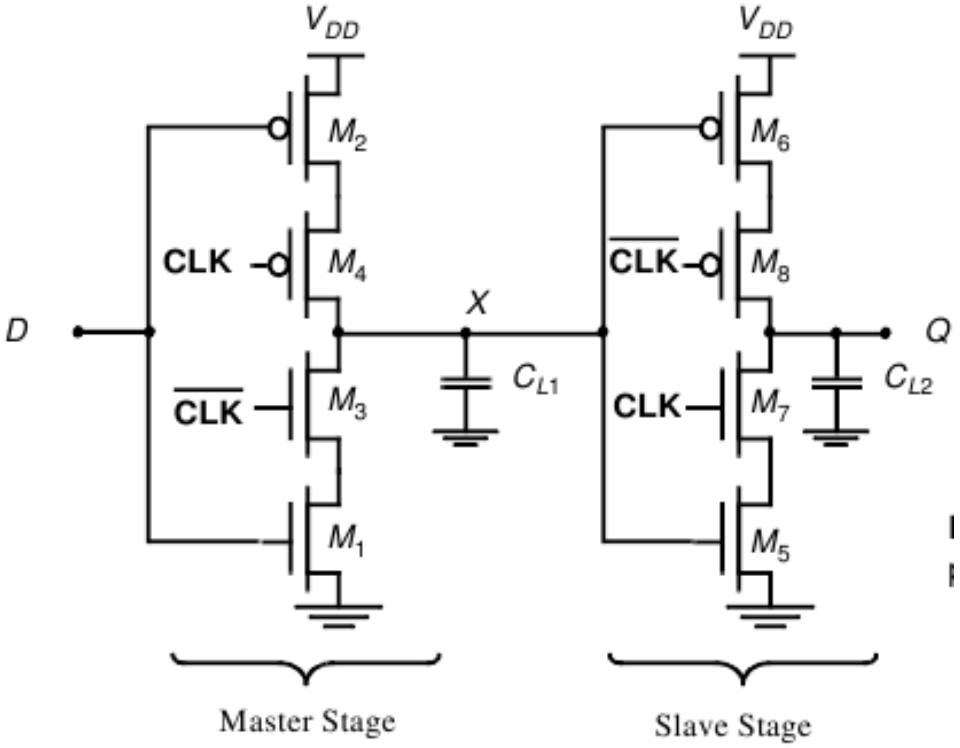


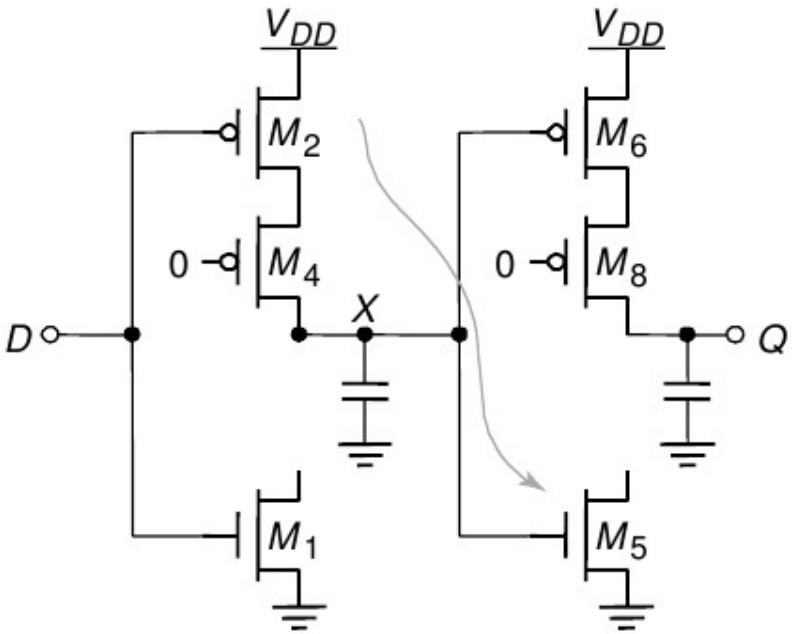
Flip-Flops Dinâmicos



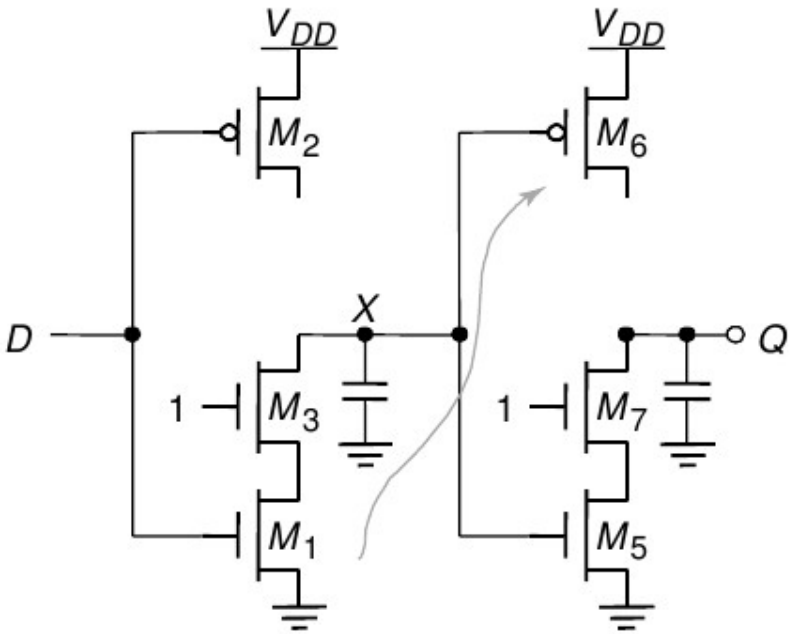
Flip-Flop Dinâmico Insensível à sobreposição do clock

C^2MOS





(a) (0-0) overlap



(b) (1-1) overlap