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DESIGN AND ANALYSIS OF N-PATH CIRCUITS

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DESIGN AND ANALYSIS OF N-PATH CIRCUITS

Projeto apresentado como requisito à obtenção de nota da disciplina de Trabalho de Conclusão de Curso A, do Curso de Engenharia Elétrica com Ênfase Eletrotécnica e Eletrônica & Telecomunicações

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RESUMO

Atualmente, diante da evolução de dispositivos hiperconectados, diversos padrões de comunicação devem ser cobertos por um único dispositivo. Além do mais, a banda passante utilizada aumenta cada vez mais, enquanto o canal utilizado permanece quase imutável. Isso resulta na necessidade de filtros de fator de qualidade elevado. As soluções implementadas hoje são, em geral, compostas de filtros não-integráveis. Com o avanço das tecnologias do tipo CMOS permitem a implementação de uma solução antiga, os filtros do tipo N caminhos. Esse filtro permite reconfiguração de sua frequência à partir de múltiplos pulsos quadrados defasados. O fator de qualidade desse filtro, teoricamente, é independente da qualidade dos componentes passivos utilizados. Todavia, há ainda inconvenientes na utilização desse filtro, o que é objeto de pesquisa. Um desses inconvenientes é a linearidade dentro da banda do filtro, que não é elevada. O trabalho aqui apresentado tem como objetivo, inicialmente, fazer o projeto dos pulsos quadrados defasados necessários, então estudar e validar os modelos matemáticos existentes. Finalmente, implementar um circuito N caminhos em paralelo com um amplificador de baixo ruído. A combinação desses circuitos permite uma alta linearidade dentro da banda passante do circuito, apresentando uma linearidade IIP_3 de 7 dBm junto com desempenho no estado da arte para as outras características do circuito.

Palavras-chave: Circuitos N caminhos, reconfiguração, integração, filtragem com Q elevado, alta linearidade

ABSTRACT

With the growth of hyper-connected devices, the number of communication standards that need to be covered by one device increases. Even further, the bandwidth covered by each channel tends to increase while the channel of each standard keeps increasing slightly. Therefore, high quality factor (Q) filters are required in communicating devices. Today's solutions for those filters require multiple non-integrable filters and this number becomes even higher by adding redundant paths for communication. To overcome those issues, the most recent CMOS nodes enable the use of an old solution, the N-Path filter. This filter's center frequency can be tuned with its clock, that should be a non-overlapping clock with N phases, while having a Q that is not dependent on its passive's Q. However, this circuit is still very sensitive to imperfections and recent works have tried to make this type of circuit robust. Furthermore, despite the great evolution presented by this circuit, no work seems to address the in-band linearity of such filters. This work aims firstly at designing the required non-overlapping clocks and then at studying and validating the existing models for N-Path filters. Afterwards, it studies the advantages of some proposed solutions to address the imperfections of the circuit. The main objective being the implementation of a LNA in parallel with a N-Path notch filter, where the LNA compensates some of the imperfections of N-Path circuits while also ensuring a high in-band linearity. The implemented circuit presents high in-band linearity while keeping similar or better performances for NF, filter rejection and power consumption, compared to the current state-of-the-art (SoA) circuits. It presents an in-band linearity IIP_3 of 7 dBm, with a 2.9 dB of NF and a 26 dB of rejection, while maintaining a in-band gain of 19 dB.

Keywords: N-Path circuits, reconfigurability, integrability, high Q filtering, multi-standards, high linearity.

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CHAPTER 1

INTRODUCTION

In recent years, the number of communication standards supported by a single hyper-connected device increased. Today a single device such as a smartphone should be able to support at least 10 different standards over 30 different frequency bands (De Souza; MARIANO; TARIS, 2017) calling for multi-standard circuits. This trend creates a highly competitive market for RF components, valued at USD 18.06 billion in 2018 and which is estimated to have a Compound Annual Growth Rate (CAGR) of 14% from 2019 to 2025 (RESEARCH, 2019). Today's solutions present multiple narrow-band radio frequency (RF) (see figure 1.1) receivers, with multiple-chips. Furthermore, to ensure reliability, redundant RF Chains are used. This approach presents no flexibility due to pre-fixed RF bandwidths (BW) and leads to high production cost as well as high power consumption.

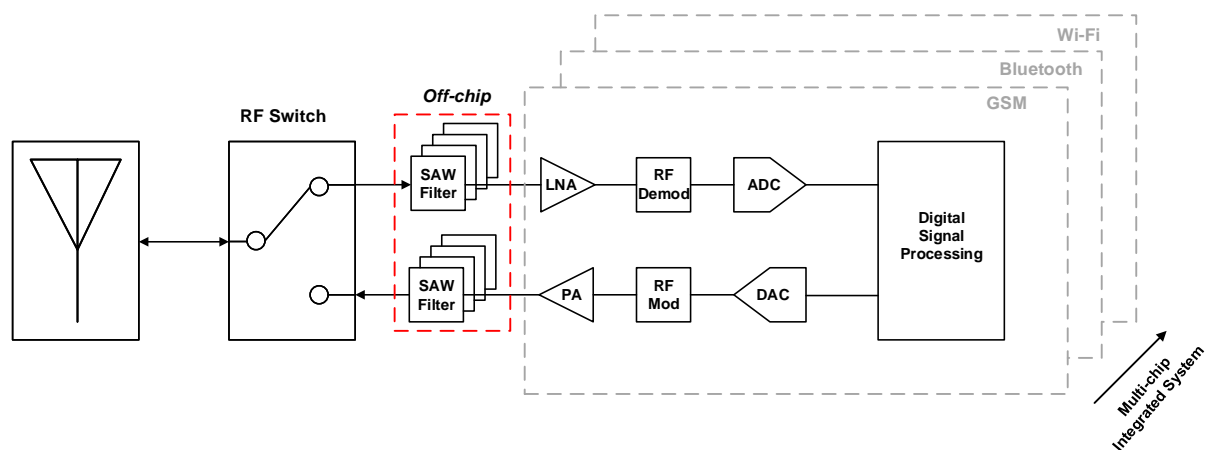


Figure 1.1: Current Multi-chip approach.

This issue has been first addressed by Mitola (MITOLA; EVOLUTION, 1995) with the concept of Software Radio (SR) (see figure 1.2 for a receiver (Rx) architecture). Figure 1.3 shows how this concept is already implemented for applications such as testing, base station for satellite missions or even amateur-radio.

However, those products are still expensive (ETTUS,), power consuming and have a large footprint.

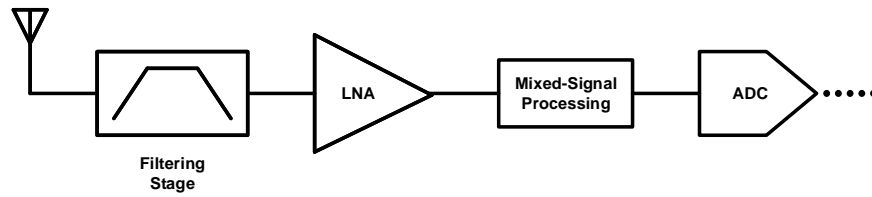


Figure 1.2: SR receiver proposed by Mitola.

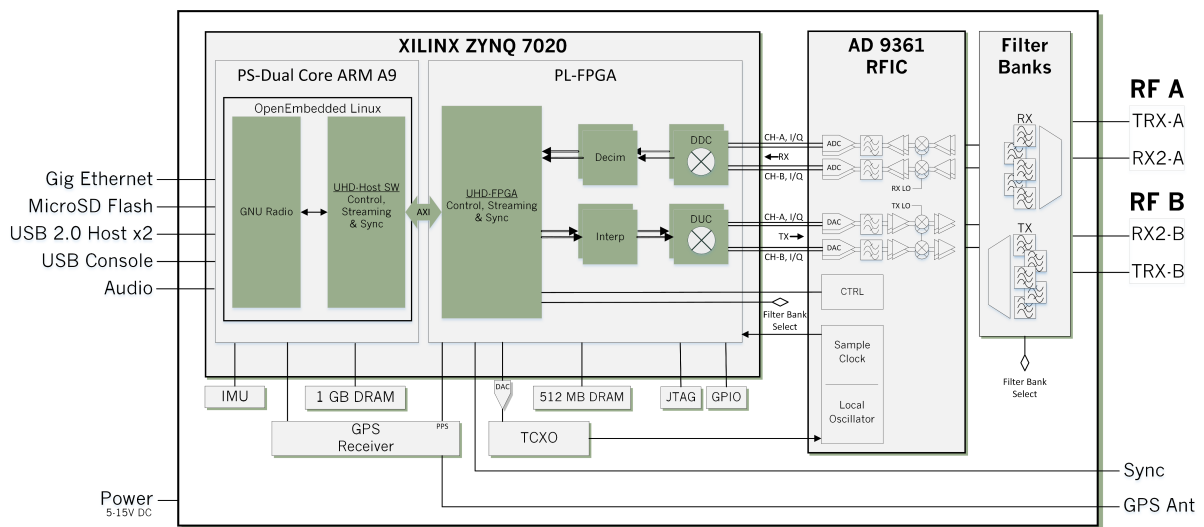


Figure 1.3: E310 USRP Architecture.

Besides, the Rx RF Front-End (RFFE) is reconfigurable for wide bandwidth and integrable into a single chip, but the RF filtering is not, as shown in the *filter Banks* of figure 1.3. This becomes even more important for small form factor devices such as in mobile phones. This filter is required to properly select the frequency allocation of the standard, for instance, 20 MHz at 2.4 GHz for Wi-Fi applications. As a result of the high amount of standards and usage of the frequency spectrum (see figure 1.4), the filters for band selection must be able to cover a relatively narrow-band while being centered at high frequencies, thus requiring a high quality coefficient (Q). For the Wi-Fi, the required Q is given by:

$$Q_{\text{Wi-Fi}} = \frac{f_c}{\Delta f} = \frac{2.4 \text{ GHz}}{20 \text{ MHz}} = 120, \quad (1.1)$$

where f_c is the center frequency and Δ_f is the channel bandwidth.

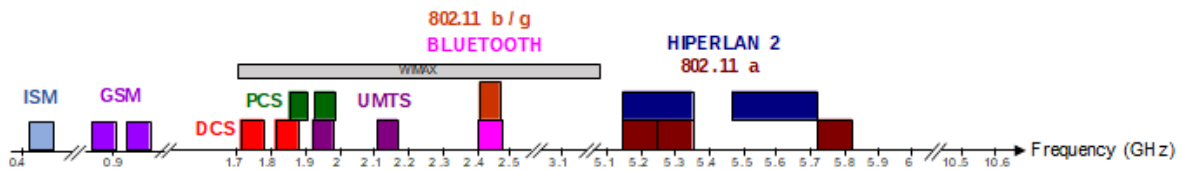


Figure 1.4: Example of some standards from 400 MHz to 6 GHz.

Currently, this narrow-band filtering is achieved through LC filters, G_m -C filters, Surface Acoustic Waves (SAW) or Bulk Acoustic Waves (BAW) filters. Each of these blocks has its own trade-offs between integrability and reconfigurability. As depicted in (DARVISHI,), while SAW/BAW filters have high Q, the first cannot be integrated and the second, while possible to be integrated into the package, has its center frequency sensitive to the thickness variation of the piezoelectric material. Regarding LC filters and G_m -C filters, they are integrable to the system-on-chip (SoC). However, the first does not obey the process scaling and has a poor Q and the second suffers from the trade-offs between the quality factor, power consumption, center frequency and dynamic range of the circuit. Therefore, even if the other blocks of the Rx RFFE are fully reconfigurable, a solution for the RF filters need to be addressed for both integration and reconfigurability.

Recently N-Path filtering (see figure 1.5 for a 4-Path filter example), which consists of N parallel paths of commuted capacitors controlled by non-overlapping clocks, has been considered to address this purpose. While it is not a novel solution, it benefits from the process scaling of CMOS technology. As this technology continues to follow Moore's law, it offers faster digital circuits and better switches (smaller on mode resistance R_{SW} and parasitic capacitance) (KLUMPERINK; WESTERVELD; NAUTA, 2017). N-Path filters are capable of integration in a SoC, reconfiguration of the center frequency and high Q due to the filter bandwidth being independent of its center frequency, its bandwidth is given by,

$$BW_{-3dB} = \frac{1}{2\pi NR_S C}, \quad (1.2)$$

where R_S is the impedance seen by the input of the circuit, N is the number of paths in the circuit and C is the capacitance presented at each path.

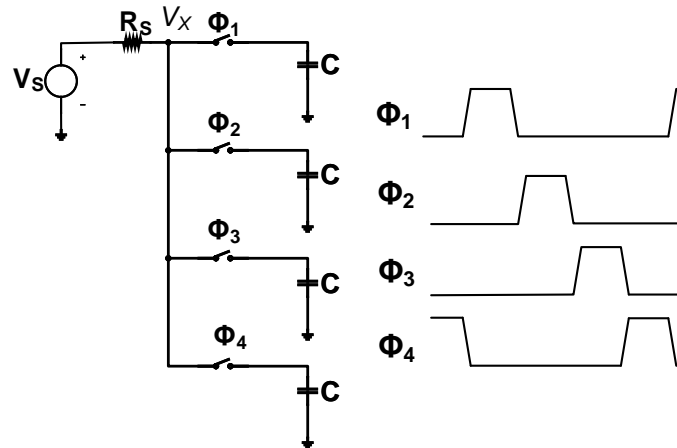


Figure 1.5: Example of a 4-Path filter and its required non-overlapping clocks to drive the switches.

In (KLUMPERINK; WESTERVELD; NAUTA, 2017), the main contributions of the state of the art are revised and discussed. This reference is the starting point of the present work. Here, the interesting property of a receiver using an LNA in parallel with an N -path notch filter, also called the "Miller Bandpass filter" (MBPF) (PARK; RAZAVI, 2014), is used as the main core of this work (see figure 1.6). The LNA block was originally developed in (De Souza; MARIANO; TARIS, 2017), it is composed of a current-reuse (CR) configuration to achieve a high voltage gain, combined with an active shunt feedback path to perform input matching and inter-modulation cancellation.

In order to address the challenges of blocker filtering and band selection mentioned in this introduction, the implementation of the LNA combined to the N -path notch filter enables a high in-band linearity while ensuring reconfiguration of the center frequency over the wide bandwidth of the LNA (0 to 6 GHz). This work presents the modelling and co-sizing of all the blocks of this circuit (clock, filter and amplifier) in 28 nm FD-SOI from ST Microelectronics. It is organized as follows: chapter 2 presents the design of the non-overlapping clock, its advantages and an optimization proposed

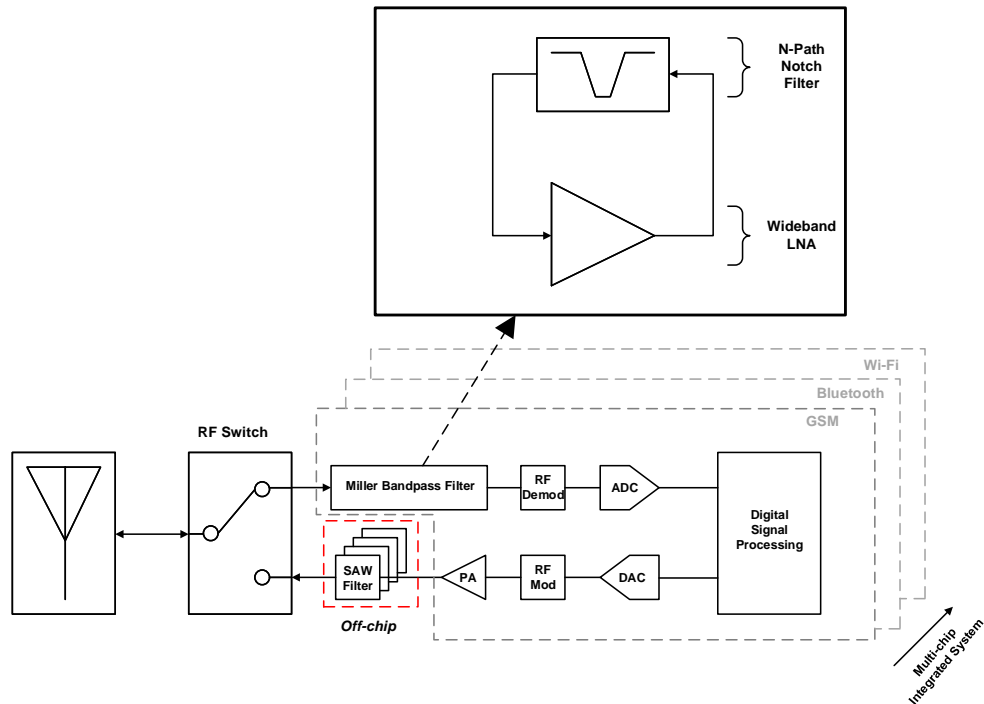


Figure 1.6: New Rx Channel with the proposed solution.

by (PARK; RAZAVI, 2014) for the clock presented by (ANDREWS; MOLNAR, 2010; YANG; YÜKSEL; MOLNAR, 2015). Chapter 3 presents the basic concepts of N-Path circuits and the validation of an analytic model by CAD simulations. Chapter 4 displays implementations of N-Path filters and the behaviour of the Miller Bandpass filter with a comparison of the results. Finally 5 presents the conclusions and some perspectives for future work. The methodology used is not explicitly exposed in a chapter, to create a more natural flow of the reading and understanding the methodology used is embedded in the chapters with the simulation setup.

1.1 OBJECTIVES

1.1.1 Main Objective

The main objective of this work is to analyze and implement multiple solutions of N-Path Circuits. Even further, the required driving circuit will be implemented. While equivalent models of this type of circuit already exist, the trade-offs of the equations are not easily

seen. This will be also studied.

1.1.2 Specific Objectives

- Analyze and validate the current mathematical models of N-Path circuits
- Implement the combination of a N-Path filter in parallel with an LNA.

CHAPTER 2

CLOCK SHAPING CIRCUIT

An N-path filter consists of N parallel paths which must be ON one at a time. Therefore, its driving circuit must be a non-overlapping clock with a duty cycle equal to $100/N\%$. Thanks to the reduction of the gate's channel length, higher frequencies can be achieved by these non-overlapping clocks in 28 nm FD-SOI. Generally, an external Local Oscillator (LO) is used, while the generation of each required phase is composed by digital circuitry. Works such as (KLUMPERINK; WESTERVELD; NAUTA, 2017) generally employ ring counters (see figure 2.1a) requiring an external LO and a frequency N times higher than the output clock frequency. Delay Locked-Loops (DLL) could also be used for this clock generation. There are multiple approaches that can be used, but because the main core of this project is the N-Path filtering, the elegant approach of (ANDREWS; MOLNAR, 2010; YANG; YÜKSEL; MOLNAR, 2015) using AND ports (see figure 2.1b) is implemented. In this chapter, two clock generation circuits are proposed: first, a 25% duty cycle non-overlapping clocks and then a 12.5% duty cycle non-overlapping clock for a 4-path filter and an 8-path filter, respectively. These circuits are derived from (ANDREWS; MOLNAR, 2010; YANG; YÜKSEL; MOLNAR, 2015), adapted by (PARK; RAZAVI, 2014).

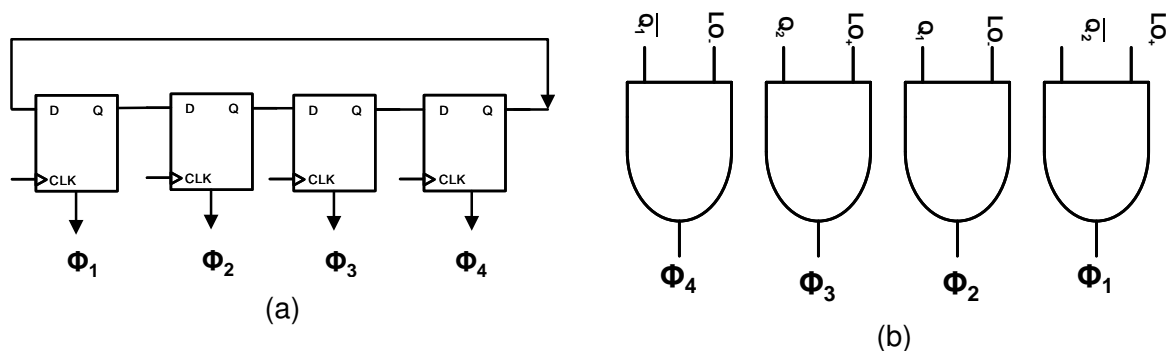


Figure 2.1: (a) Ring counter with N times input frequency, (b) proposed clock generation circuit both for a 4-Path filter.

2.1 25% Duty Cycle Non-overlapping Clocks

The circuit proposed by (ANDREWS; MOLNAR, 2010; YANG; YÜKSEL; MOLNAR, 2015) (see figure ??) supposes a differential LO for the reference frequency, one could have the same by simply adding an inverter at the output of a single-ended LO. The LO frequency is divided by two, using a divider by two counter, which is a D flip-flop with its \bar{Q} output connected to its D input. Figure 2.2b presents the implementation of the divider by two using D latches.

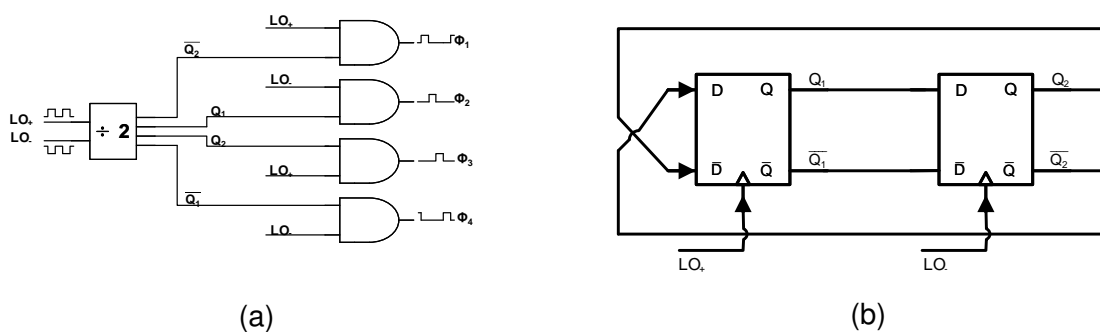


Figure 2.2: (a) Logic circuit used, (b) generation of 4 phases using D type latches.

This circuit creates by itself four signals: Q_1 , \bar{Q}_1 , Q_2 , \bar{Q}_2 . Naturally, this creates four 50% duty cycle signals, phased by 90° from each other. For a precise analysis, a small delay between the generated signals and the LO is taken into account. Then, the LO signal is added with Q_1 , \bar{Q}_1 , Q_2 , \bar{Q}_2 signals by using AND ports and using the correct logic table. For instance, if the signal Q_1 has the logic level '1' and the LO_- signal has the logic level '1' at the same time, a resulting signal, Φ_2 has the logic level '1', but if any of the signals Q_1 or LO_- has the logic level '0', the signal Φ_2 has the logic level '0'. The complete system with all signals is presented in figure 2.2a, where the digital logic is shown in figure 2.3 with its transistor-level circuit of each logic block. This circuit has two advantages: 1) the output frequency of the signals is equal to the external LO frequency, 2) the pulse edge is insensitive to deviations of the counter (ANDREWS; MOLNAR, 2010). Instead of the logic table, figure 2.4 allows a direct visualization of the logic presented in figure 2.2a.

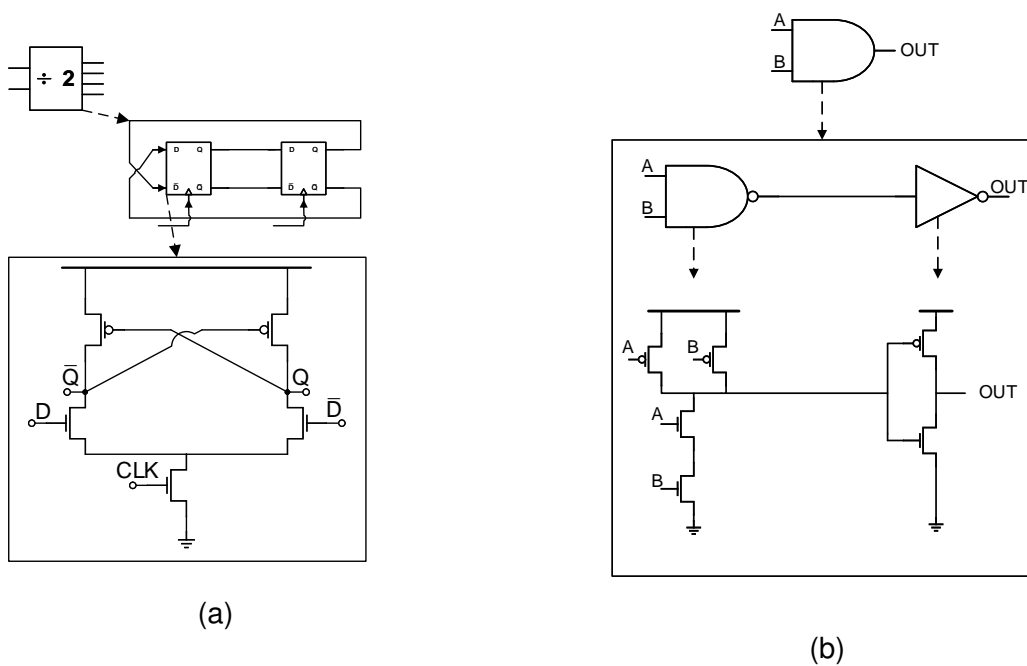


Figure 2.3: (a) type D latch used for the divider by two circuit, (b) AND circuit composed by a NAND and a NOT gate.

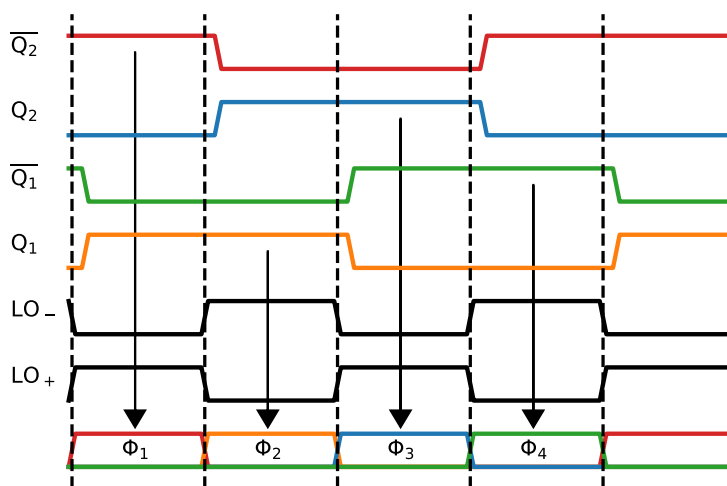


Figure 2.4: Signal Diagram for the 25% Duty Cycle Non-overlapping Clocks.

2.2 12.5% Duty Cycle Non-overlapping Clocks

The strategy for the generation of eight phases (12.5% duty cycle clock) is similar to the four phases generation presented in the previous section except the divider by four which is based on a Johnson Counter, as shown in figure 2.5b) (ANDREWS; MOLNAR, 2010; YANG; YÜKSEL; MOLNAR, 2015). This arrangement allows to generate eight signals $Q_1, \overline{Q_1}, \dots, Q_4, \overline{Q_4}$ (see figure 2.5a for the non-inverted signals). Those outputs can be combined by using AND ports to create eight 25% duty cycle pulses split by 45° , the logic circuit is shown in figure 2.6, while the signal diagram of figure 2.7 shows the logic to generate two of those pulses.

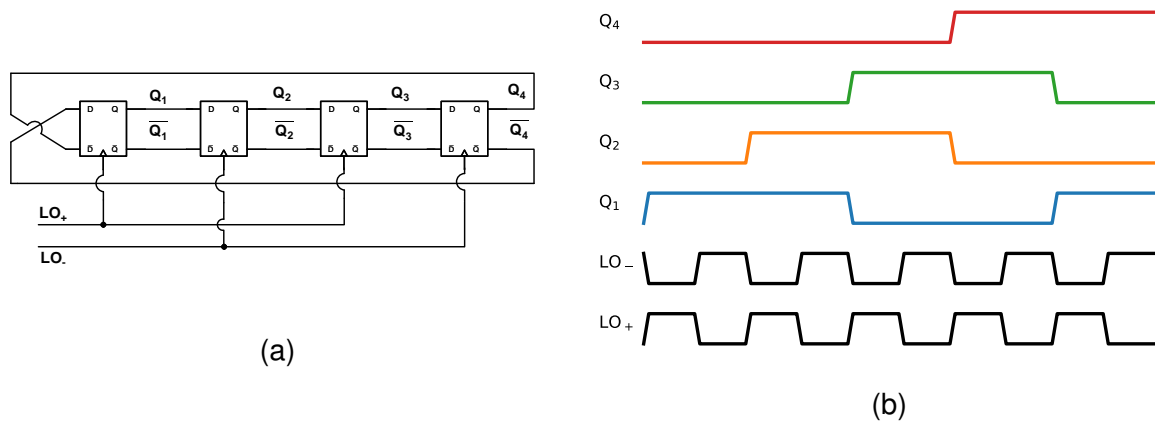


Figure 2.5: (a) Johnson counter and its outputs (using D type Latches), (b) Johnson counter signal diagram.

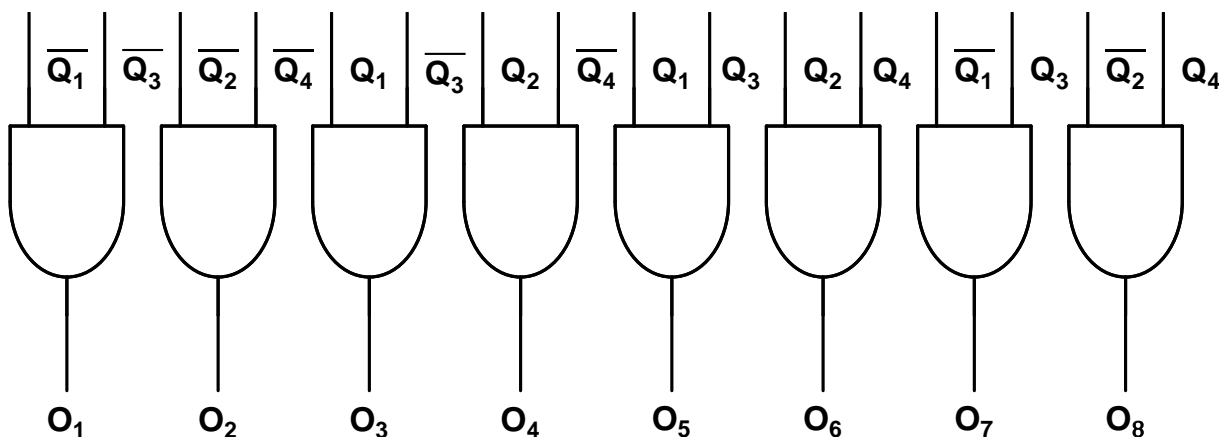


Figure 2.6: Logic combination for 25% duty cycle pulses split by 45°

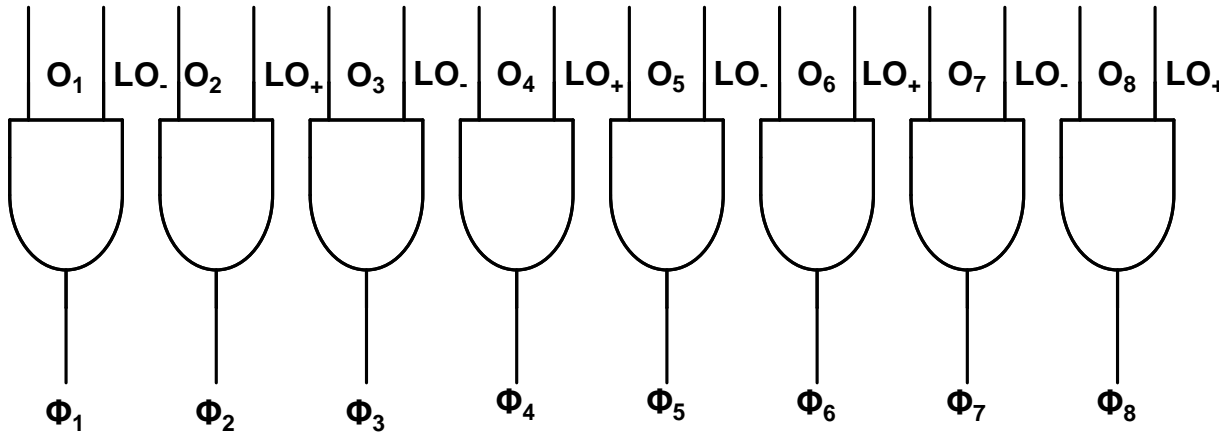


Figure 2.7: Signal diagram for 12.5% duty cycle pulses split by 45° .

Those pulses can again be combined, now with the LO signal, to create eight 12.5% duty cycle pulses also split by 45° , creating the desired non-overlapping clock. The circuit is shown in figure 2.7, while the signal diagram of two of the generated clocks is shown in figure 2.8.

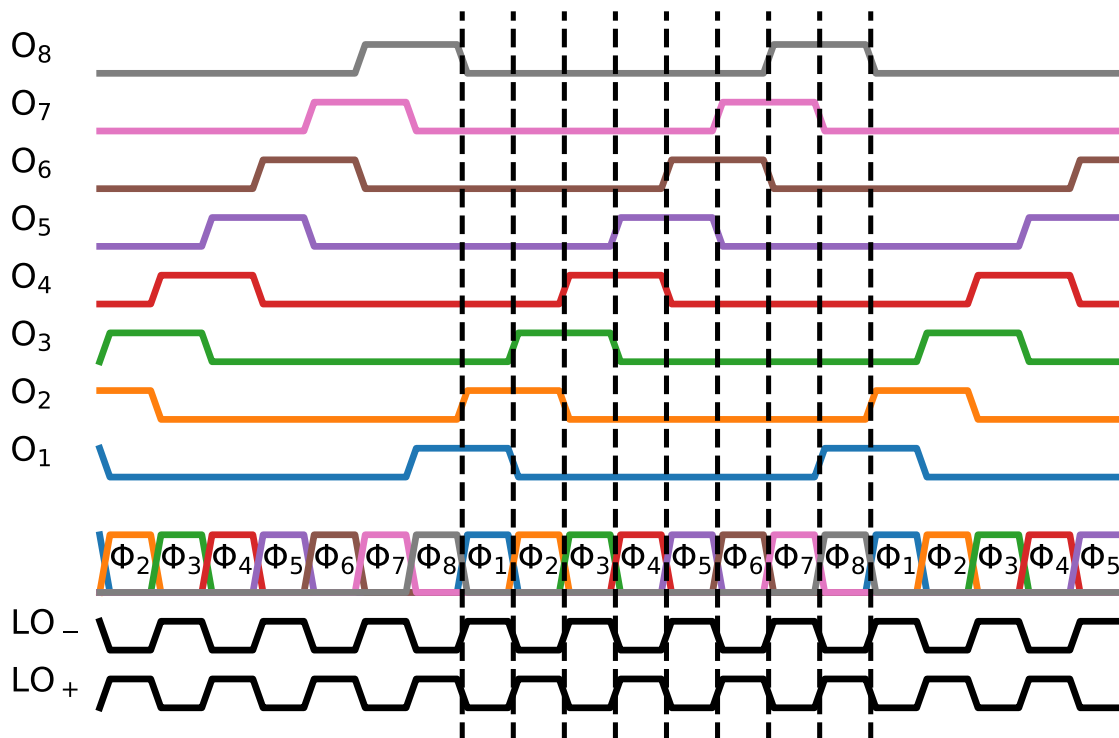


Figure 2.8: Signal Diagram for 12.5% Duty Non-overlapping Clocks.

Now, instead of generating those pulses using 16 2-Input AND ports, we could use 8 3-Input AND ports, as proposed by (PARK; RAZAVI, 2014). While (PARK;

RAZAVI, 2014) optimizes the transistor-level design and uses drain sharing, this work only uses the digital logic behind it (see figure 2.9) for the circuit.

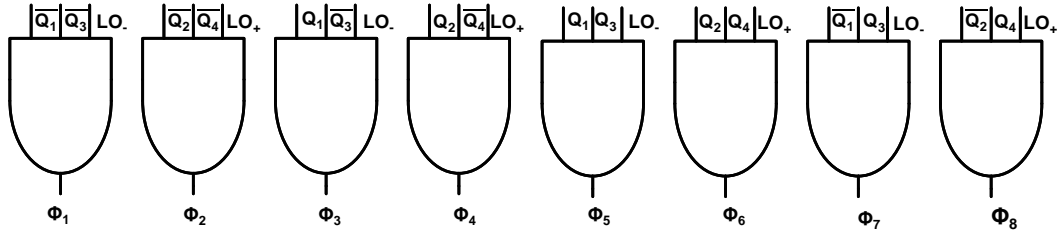


Figure 2.9: Digital circuit used to generate the 12.5% non-overlapping clocks.

2.3 Simulation Results

This section shows the simulation results for the circuits. These circuits were designed using the ST Microelectronics 28 nm FD-SOI technology. The sizing is further explained in the appendix A. A large number of simulations were realized to test the limits of the circuit, its consumption and the optimization for multiple fan-outs. The fan-out is the maximum load that can be connected to the output of a logic circuit, in this work the fan-out is a function of the capacitive load presented by the gate of the transistors used as a switch and the number of switches used. The simulator used was SpectreRF, using transient simulations.

2.3.1 25% Duty Cycle Non-overlapping Clocks

The simulated setup is illustrated in figure 2.10. The LO is simulated with a pulse generator, the frequency of both LO_+ and LO_- is the same and it varies from 400 MHz to 8 GHz, a 30% margin is taken into account for future post-layout and layout parasitics due the connections between transistors, its overlapping (creating parasitic capacitors). The width of the transistor used as charge (to simulate the fan-out) varies from $10 \mu\text{m}$ to $120 \mu\text{m}$ to simulate the size of the transistor that might be implemented.

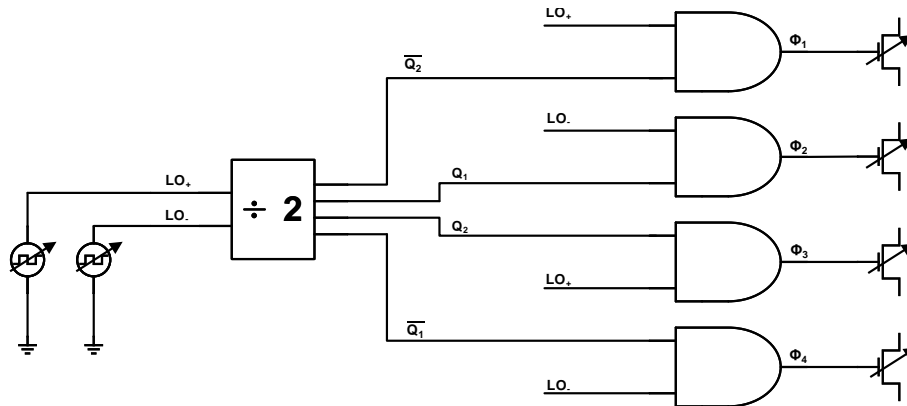


Figure 2.10: Simulation setup for the 25% Non-overlapping Clock Generation.

Figure 2.11a shows the waveform of the divider by two and figure 2.11b shows the 25% duty cycle non-overlapping clocks. The frequency of the LOs is 2 GHz, while the size of the charge transistor is $120\ \mu\text{m}$, this represents the worst case scenario. As one can see, the given result is almost the same as the theoretical plots, with some glitches due to the parasitic capacitances presented by the transistors. Those glitches become even more apparent with the increase of the LOs frequency. Furthermore, figure 2.11a displays the 25% duty cycle non-overlapping clocks, here the glitches are minimized because the inverter acts as a buffer. This cleans the glitches presented in the previous stages.

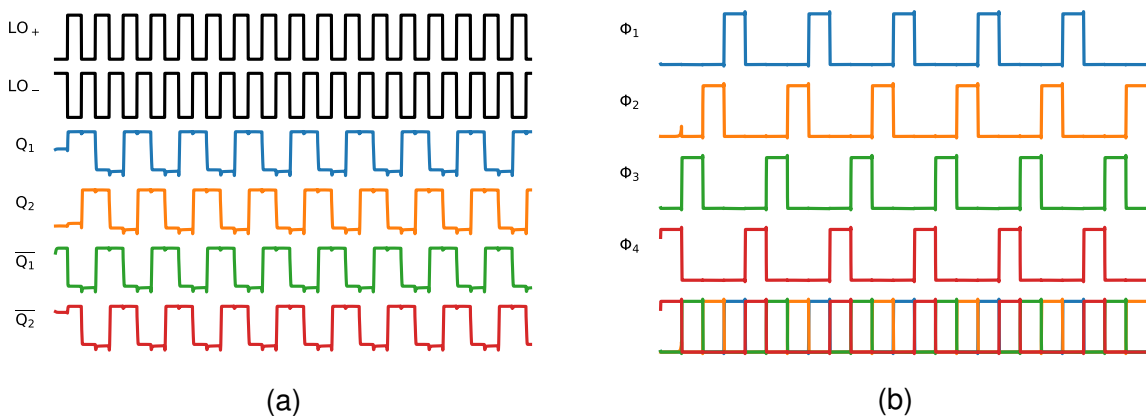


Figure 2.11: (a) Simulated divide by two circuit, (b) simulated 25% Duty Cycle Non-overlapping Clocks.

2.3.2 12.5% Duty Cycle Non-overlapping Clocks

The simulation setup is the same as for the 25% duty cycle non-overlapping clocks with the frequency of the LOs varying from 400 MHz to 8 GHz and the width of the charge transistors varying from $10\ \mu\text{m}$ to $120\ \mu\text{m}$. Figure 2.12a shows the simulated results for the Johnson counter, figure 2.12b shows the 25% duty cycle pulses split by 45° and finally figure 2.12c shows the 12.5% duty cycle non-overlapping clocks, with LOs frequency at 2 GHz and $120\ \mu\text{m}$ transistors. It is important to notice that the intermediary stage of figure 2.12b is only simulated but not truly implemented, because of the optimization proposed and presented in figure 2.9. However, this simulation is part of this work because it creates a sequential thinking sequence. The glitch presented in figure 2.12a disappears in the intermediary level (figure 2.12b).

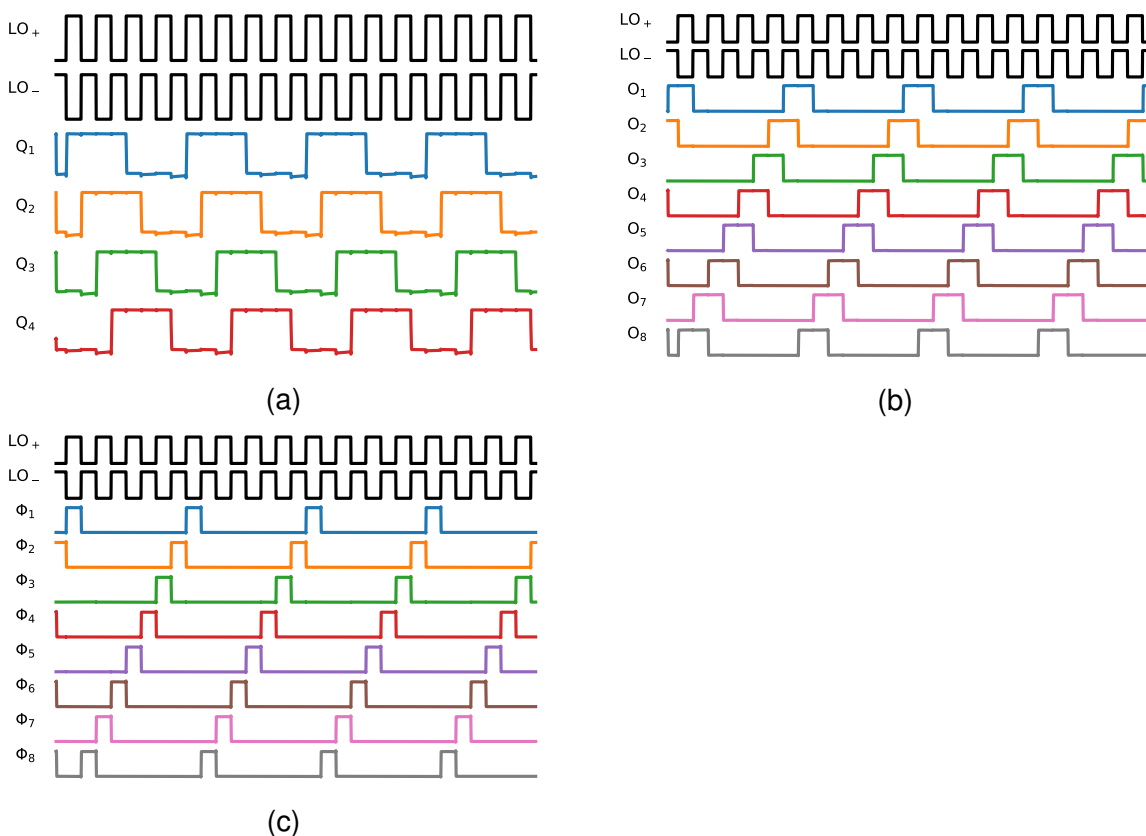


Figure 2.12: (a) Simulated Johnson counter, (b) simulated 25% duty cycle pulses split by 45° , (c) simulated 12.5% Duty Cycle Non-overlapping Clocks.

2.4 Circuit Power Consumption

For both circuits, there are two currents that are drained: one from the DC biasing and one from the external LO. The first one is the actual consumption of the circuit and the second sets the maximal power that the LOs should be able to deliver to the circuit. These currents have a periodic and time variant behaviour, but the average level of the latter is close to zero, thus it is not taken into account here. Figure 2.13 illustrates the simulated waveform of the current. To determine the power consumption of the circuit, the average of this current should be calculated over a long period of time to minimize errors. The biasing voltage is equal to 1 V, so the power consumption is directly calculated from the current waveform. In this case, the average consumption is equal to 7.4 mW. Furthermore, the plot displayed in figure 2.14 assembles the power consumption for the possible N-Path circuits to be used, presenting a minimal power consumption of 716 μ W and a maximal power consumption of 5.74 mW. It should be noted that the power consumption clearly increases by: 1) having a bigger switch and thus a bigger capacitive load, 2) increasing the frequency.

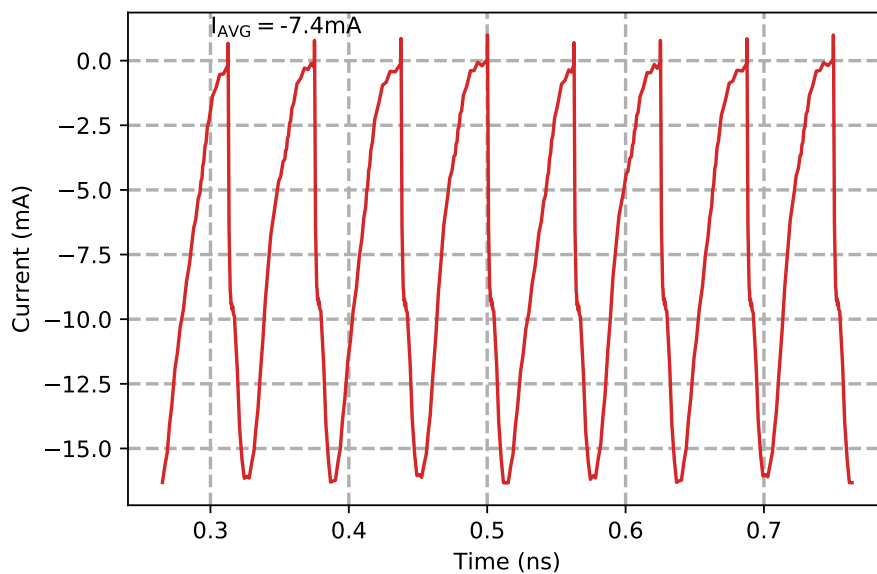


Figure 2.13: Simulated current waveform for the bias circuit.

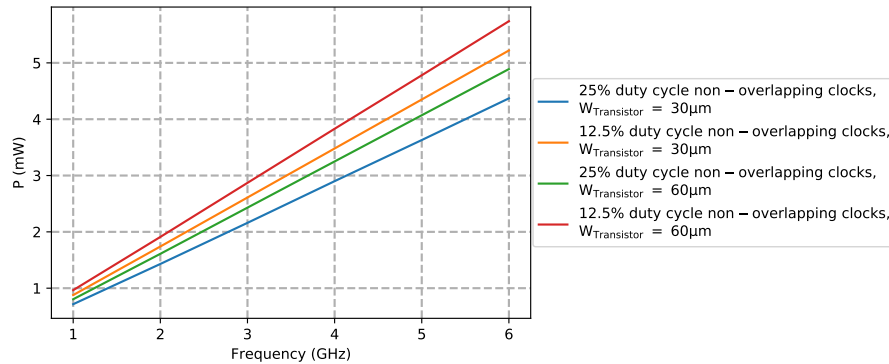


Figure 2.14: Current consumption of the circuit for multiple cases.

2.5 Conclusion

This chapter demonstrates that a simple solution using digital logic can be used to create non-overlapping clocks with duty cycle of $100/N\%$. Most of the clock generation proposed in the literature require an external LO with a frequency N times higher than the output frequency. This limits the maximum achievable frequency. The presented solution, throughout a specific approach of logic gate combination, allows the generation of 4 and 8 phase output clocks at the same frequency as the external LO. Besides, the 28 nm FD-SOI technology enables the polarization of the back-gate. This can reduce even more the power consumption. The proposed solution presents higher achievable frequencies while having a smaller power consumption, compared to the majority of circuit employed in recent N-Path circuits (KLUMPERINK; WESTERVELD; NAUTA, 2017).

CHAPTER 3

N-PATH CIRCUITS

As illustrated by (KLUMPERINK; WESTERVELD; NAUTA, 2017), N-Path Circuits are long known dating from the early 1950s with the first description of the behaviour of N-Path Filters being given by (SMITH,). This type of circuit has had multiple names historically, this works keeps the actual trend of using the term "N-Path". The bandwidth of such circuits is given by equation (1.2, in chapter 1). They consist of a first-order RC circuit (which can be implemented as low or high-pass), where the capacitor is replaced by an array of N commuted capacitors. Each capacitor is connected to the output node one by one, with a time rate of f_R (see figure 3.1a). Today this commuted network is composed of switches driven by non-overlapping clocks (see figure 3.1b).

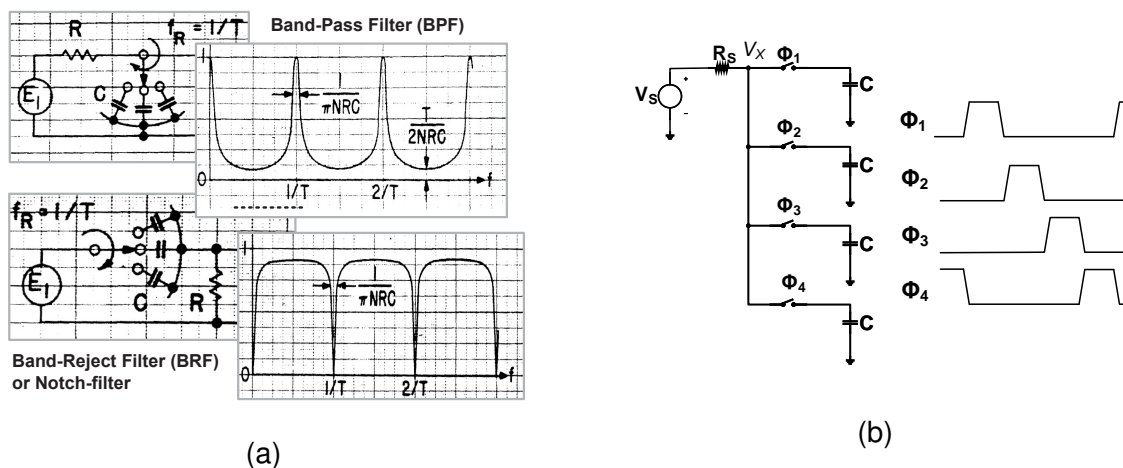


Figure 3.1: (a) Commuted network [6], (b) 4-Path band-pass filter using switches and its driving non-overlapping clocks.

3.1 Time Domain Behaviour

Consider a sinusoidal waveform with a signal frequency of f_s injected into the 4-Path circuit through the voltage source V_S as illustrated in figure 3.2. All the components are assumed ideal (switches and capacitors) while the source presents a resistance R_S . It is also assumed that:

$$R_S C \gg T_{ON}, \quad (3.1)$$

where C is the value of each capacitor and T_{ON} is the time the switch is kept closed.

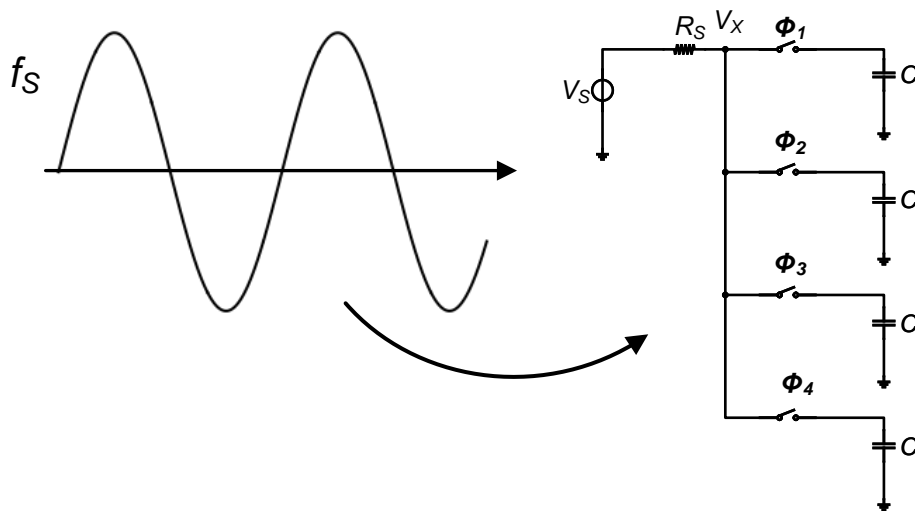


Figure 3.2: Injected signal and circuit.

When the switching frequency f (T_{ON}^{-1}) is equal to the signal frequency f_s (as shown in figure 3.3), a part of the signal (here 1/4) passes through each path. The capacitors are charged with the average of the signal that went through the path. Because of the periodicity of this process, the voltage seen by each capacitor is always the same. Thus the voltage at node V_X is a pseudo-sine created by the average voltage stored by the capacitors, this is commonly called by stair-cased sine (see figure 3.3).

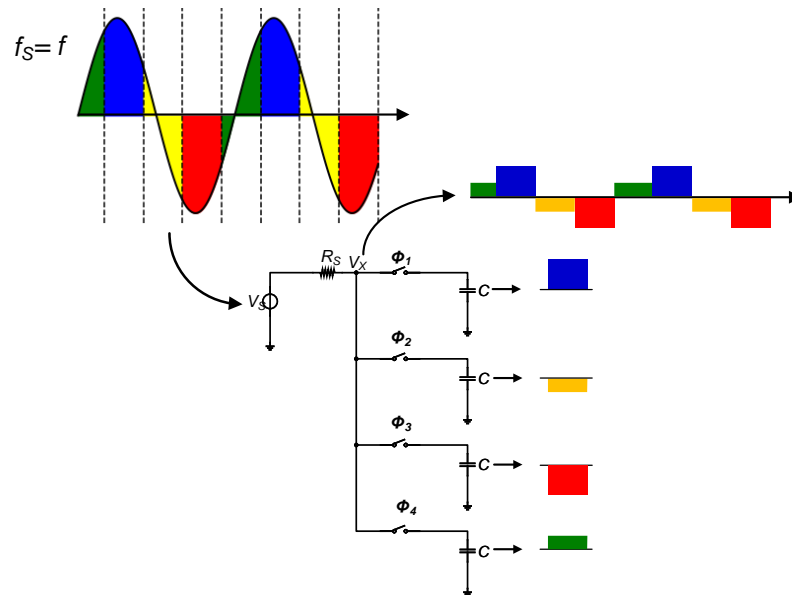


Figure 3.3: Temporal response of the circuit with $f_s = f$.

Now we assume that the signal frequency is not the same as the switching, i.e. $f_s = 1.5f$. As is shown in figure 3.4, each capacitor sees a different part of the signal, thus the average voltage is zero. Hence, for signal frequencies close to the switching frequencies, the voltage presented at the node V_x is almost the same as the one presented by the signal. Contrarily if the frequency of the signal is not the same as the switching frequency, the voltage at node V_x is equal to zero.

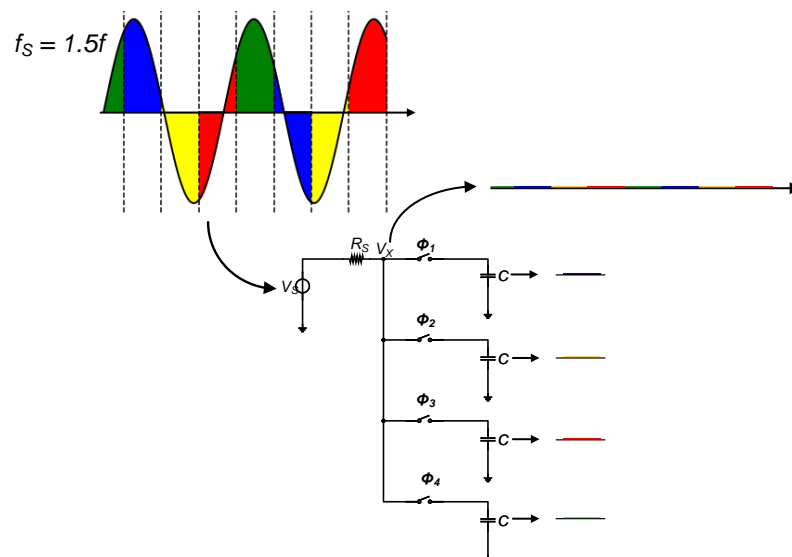


Figure 3.4: Temporal response of the circuit with $f_s = 1.5f$.

One last property of this circuit that can be well illustrated through this analysis is the *down-folding*. This property depends on the number of paths of the circuit. A signal with a frequency $f_s = i \cdot f$ is now analyzed, where $i = kN \pm 1, k \in \mathbb{Z}$. One can see, as illustrated in figure 3.5 that now the average voltage on each capacitor is smaller than in the first case, but it is not equal to zero as for the previous case. This is the down-folding phenomena presented by the circuit. It can also be assumed that by increasing the number of paths N : 1) the signal seen at node V_X is closer to the signal of V_S , 2) the down-folding is pushed to higher frequencies. While the time domain gives a clear insight on how the circuit works and on some of its properties, it doesn't fully illustrates the behaviour of the circuit.

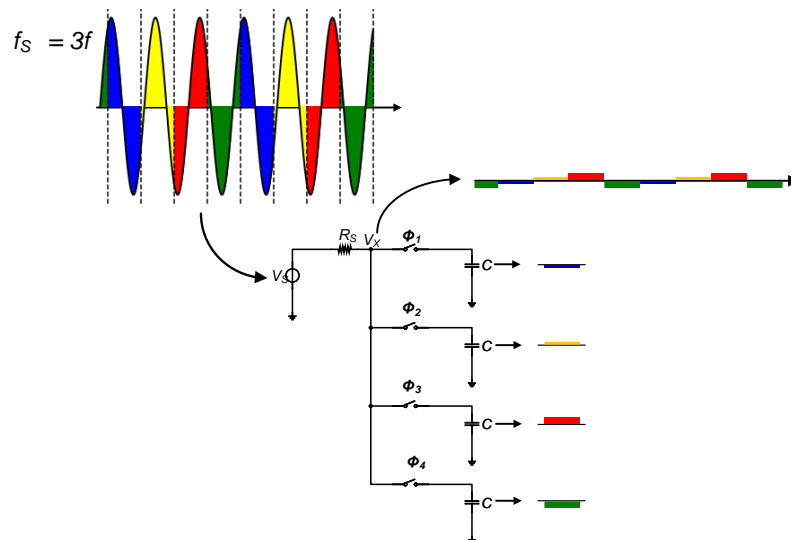


Figure 3.5: Temporal response of the circuit with $f_s = 3f$.

3.2 Frequency Domain Behaviour

In this section, the circuit presented in figure 3.2 is analyzed. For matters of simplicity and comprehension, we chose to describe a bandpass filter but this can be easily extended to a notch filter. Such circuit can be represented by two mixers and a low-pass filter, as illustrated in figure 3.6. The signal of interest (grey) is down-converted by the first mixer, filtered by the LP filter (red) and up-converted by the second mixer. As we can see a signal at $1.5f_s$ (blue) is also down-converted, but is rejected by the LP

filter. Here the down-folding is not shown, as it was in the time domain analysis. The frequency representation of this is shown in figure 3.7.

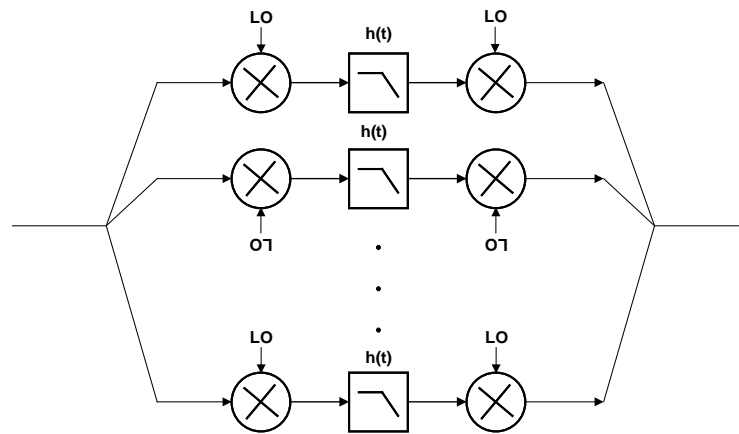


Figure 3.6: N-Path Bandpass representation using two mixers and LP filter.

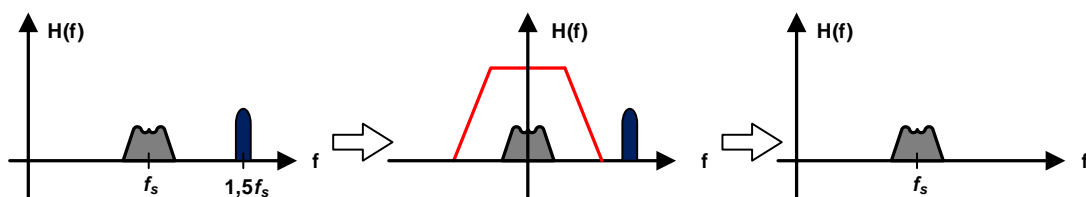


Figure 3.7: Frequency domain illustration of the two mixer and LP filter representation.

This is only true when there is a perfect multiplication of the signal of interest and a cosine. Actually, the multiplication here is from the signal of interest and a square wave, which presents harmonics. Even further, if the square wave was perfect only odd harmonics would be present, but this is not entirely true. Thus, the signal is not only multiplied by f_s , but also by each one of its integers $i \cdot f_s, i \in \mathbb{Z}$.

3.3 Mathematical Behaviour

The mathematical modelling and behaviour of N-Path circuits is by itself a research field. There are multiple approaches to describe its behaviour from its harmonic response in (DARVISHI, ; GHAFFARI et al., 2011; GHAFFARI; KLUMPERINK;

NAUTA, 2010; MIRZAEI; DARABI; MURPHY, 2012) to its noise and impedance models in (DARVISHI, ; ANDREWS; MOLNAR, 2010; GHAFARI et al., 2011; MIRZAEI; DARABI; MURPHY, 2012). In (IIZUKA; ABIDI, 2016a, 2016b; IIZUKA; ABIDI, 2016b), they formalize an unified treatment for switched R-C circuits in general, using a signal flow graph (SFG). The work in (MIRZAEI; DARABI; MURPHY, 2012) gives an accurate model of the behaviour of N-Path filters and it enables a simple visualization of the results presented in (PARK; RAZAVI, 2014; XU; ZHU; KINGET, 2014). They model the N-Path as illustrated in figure 3.8, where all the switches present a ON resistance of R_{SW} and are controlled by an N-Phase non-overlapping clock.

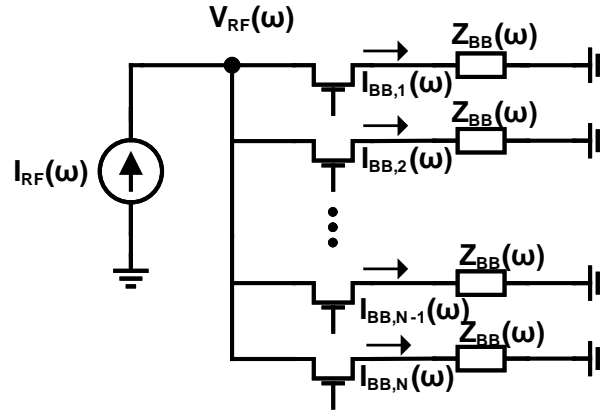


Figure 3.8: Example of generic N-Path circuit with generic baseband impedance.

We assume that the current source $I_{RF}(\omega)$ presents an infinite impedance and an N-Phase non-overlapping clock command to each switch with a period of T_{LO} . Each switch should be ON in a period of T_{LO}/N . The following equation describe the periodic function of the non-overlapping clock and its Fourier series:

$$S_i(t) = \begin{cases} 1, & kT_{LO} < t < (k + \frac{i-1}{N}) T_{LO}, k \in \mathbb{Z} \\ 0, & \text{otherwise} \end{cases} \quad (3.2)$$

$$S_i(t) = \sum_{i=-\infty}^{\infty} a_n e^{-j(i-1)n\frac{2\pi}{N}} e^{jn\omega_{LO}t} \quad (3.3)$$

where $i = 1, 2, \dots, N$, $a_n = \frac{\sin(n\frac{\pi}{N})}{n\pi} e^{jn\frac{\pi}{N}}$. There are two voltages that can be seen,

the voltage at each path that is also called the baseband voltage $v_{BB, i}(t)$ and the RF voltage $v_{RF}(t)$, given by:

$$v_{BB, i}(t) = [S_i(t)i_{RF}(t)] * z_{BB}(t). \quad (3.4)$$

$$v_{RF}(t) = R_{SW}i_{RF}(t) + \sum_{i=1}^N S_i(t)v_{BB, i}(t). \quad (3.5)$$

Now, in order to simplify all the convolution products, a Fourier transform is applied to equations (3.3), (3.4) and (3.5), respectively resulting in:

$$S_i(\omega) \sum_{i=-\infty}^{\infty} a_n e^{-j(i-1)n\frac{2\pi}{N}} \delta(\omega - n\omega_{LO}). \quad (3.6)$$

$$V_{BB, i}(\omega) = S_i(\omega)Z_{BB}(\omega - n\omega_{LO}). \quad (3.7)$$

$$v_{RF}(\omega) = R_{SW}i_{RF}(\omega) + N \sum_{n=-\infty}^{\infty} \sum_{m=-\infty}^{\infty} a_n a_m I_{RF}(\omega - (n+m)\omega_{LO}) Z_{BB}(\omega - n\omega_{LO}), \quad (3.8)$$

where $n+m = kM$, $k \in \mathbb{Z}$. From this, it should be noted that R_{SW} becomes dominant at higher frequencies offsets (from the LO frequency and its harmonics) and the equations of insertion loss and maximum rejection (for notch filters and band-pass filters, respectively) can be given by:

$$\text{Insertion Loss} = \frac{R_S}{R_S + R_{SW}} \quad (3.9)$$

$$\text{Rejection} = \frac{R_{SW}}{R_{SW} + R_S}, \quad (3.10)$$

where R_{SW} is the resistance of the switch in ON mode and R_S is the voltage source impedance at the input of the circuit (a simple source transformation can be used for

the equation (3.8)). Furthermore, equations to address the imperfections of the circuit are given below. In (XU; ZHU; KINGET, 2014), the ratio of the gain at desired signal frequency to the gain at clock harmonics, HA , is given by:

$$HA_i = \frac{\text{sinc}^2\left(\frac{\pi}{N}\right)}{\text{sinc}^2\left(\frac{i\pi}{N}\right)}, i \in \mathbb{Z}. \quad (3.11)$$

Unwanted signals at clock harmonics can be folded to the desired signal frequency. The harmonic folding rejection ratio (HFRR) is the ratio between the gain of the desired signal frequency and the gain at clock harmonics frequency and is given by:

$$HFRR_i = \frac{\text{sinc}\left(\frac{\pi}{N}\right)}{\text{sinc}\left(\frac{i\pi}{N}\right)}, i = kN \pm 1, k \in \mathbb{Z}. \quad (3.12)$$

The conversion of RF signal at each harmonic of the clock to baseband corrupts the SNR. The HRR is the ratio of the conversion gain for the desired signal and for signals at clock harmonics, given by:

$$HRR_i = \frac{\text{sinc}\left(\frac{\pi}{N}\right)}{\text{sinc}\left(\frac{i\pi}{N}\right)}, i \in \mathbb{Z}. \quad (3.13)$$

By having a differential topology, the even harmonics are cancelled (GHAFARI; KLUMPERINK; NAUTA, 2013) and thus for equations (3.11, 3.13), $i = \text{odd}$. To illustrate the trade-off in the election of the number of phases, the simulation of HA is represented in figure 3.9 for a 4-path and a 8-path band-pass filter. To improve the rejection of the filter, a 4-path should be chosen, whereas to ensure a low NF and a low insertion loss, an 8-path should be chosen.

The simulated circuits present an HA_2 of 4.3 dB and 1.4 dB for 4 and 8 path respectively. Both circuits were simulated with the same setup (R_{SW} , f_{CLK} , C). We can also see that an 8-Path Filter has a narrower band which is natural from equation (1.2).

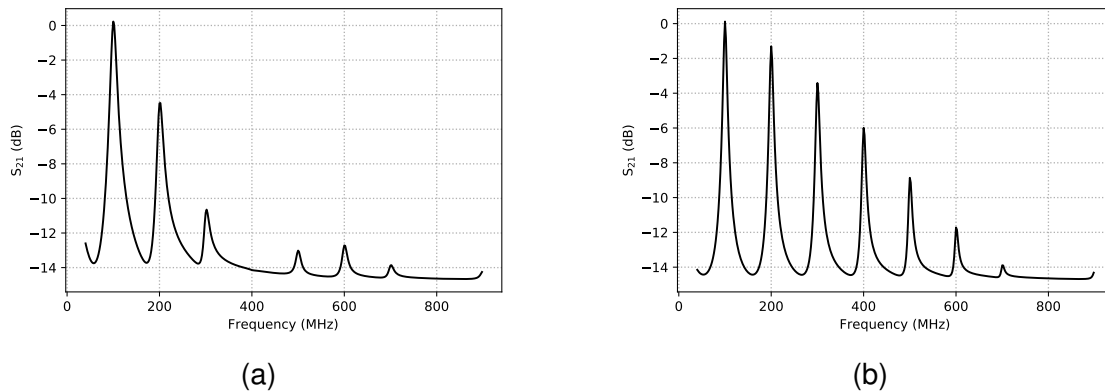


Figure 3.9: Harmonic response of: (a) 4-Path BPF with clock frequency of 100 MHz, (b) 8-Path BPF with clock frequency of 100 MHz.

3.4 Linear Time Invariant Model for N-Path Circuits

In Analog/RF design, LTI models are usually employed for circuit analysis and derivation. Because of the periodicity presented by N-Path circuit, an interesting LTI model (see figure 3.10) can be derived (ANDREWS, 2012). It fully takes into account the re-radiation of the spectrum at $(kN \pm 1)f_{LO}$, $k \in \mathbb{Z}$ frequencies (see figure 3.11). This model is further extended by (YANG; YÜKSEL; MOLNAR, 2015), creating a simple design method for both mixer-first circuits and N-Path BPF.

Model.pdf

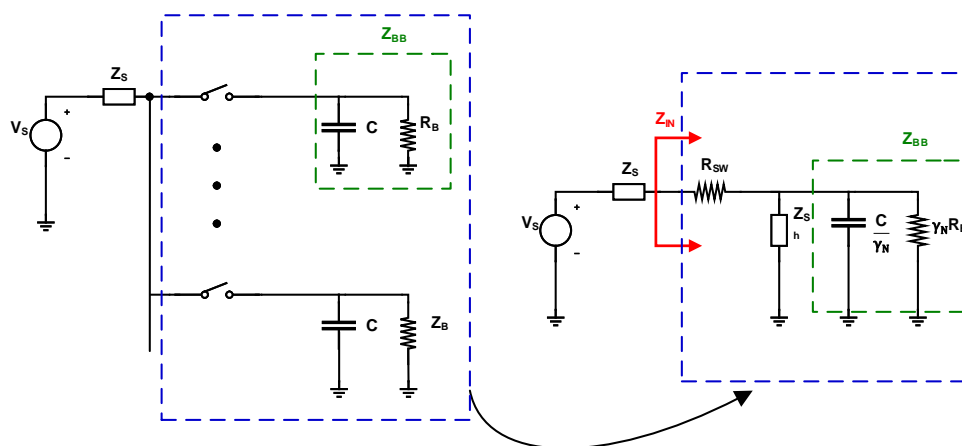


Figure 3.10: LTI Model proposed.

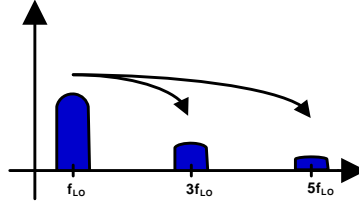


Figure 3.11: Spectrum Reradiation for a 4-Path Circuit.

This model introduces a scaling factor γ_N and a shunt impedance Z_{Sh} that models the losses due to harmonic re-radiation, the later being dependent of the scaling factor K_{N0} . It is assumed that the source impedance Z_S is real and is represented by a resistance R_S . These equations are given by:

$$\gamma_N = \frac{\text{sinc}^2\left(\frac{\pi}{N}\right)}{N}, \quad (3.14)$$

$$K_{N0} = \frac{N\gamma_N}{1 - N\gamma_N}, \quad (3.15)$$

$$Z_{Sh} = (R_s + R_{SW})K_{N0}, \quad (3.16)$$

where N is the number of paths of the circuit, R_{SW} is the ON mode resistance of the switch and R_S is the impedance of the voltage source at the input of the circuit. Now we can develop the input impedance Z_{IN} equation, given by:

$$Z_{IN} = R_{SW} + Z_{Sh} || Z_{BB}, \quad (3.17)$$

where Z_{BB} is the baseband impedance, in this case the parallel between R_B and C . For impedance matching $Z_{IN} = R_S$. Now, impedance match can be achieved through R_B such that:

$$R_B = \frac{1}{\gamma} \frac{Z_{Sh}R_S - Z_{Sh}R_{SW}}{Z_{Sh} + R_{SW} - R_S} \quad (3.18)$$

This model is verified through simulation (PSS and PSP in SpectreRF) of a 4-Path circuit, using real switches (28 nm FD-SOI transistors) with $R_{SW} \approx 5 \Omega$, $C = 200$

pF and source resistance of $R_S = 50 \Omega$. The simulation setup is shown in figure 3.12. The results are shown in figure 3.13. The first figure illustrates the real part of the input impedance Z_{IN} in function of R_B , with $f_{CLK} = 100$ MHz. Then the behaviour of equation (3.17) versus the frequency is simulated. The frequency sweep is from 85 MHz to 115 MHz with a fine tuning of the R_B sweep (from from 100 to 500 Ω) to verify if the matching impedance $R_B = 278 \Omega$ found using equation (3.18) ensures impedance matching (see figure 3.13b). Finally with a fixed $R_B = 286 \Omega$ a sweep in frequency from 85 MHz to 115 MHz to verify the real and imaginary parts of the impedance Z_{IN} is shown in figures 3.13c and 3.13d verifying the model. This was further extended for multiple values of f_{CLK} , R_{SW} and C .

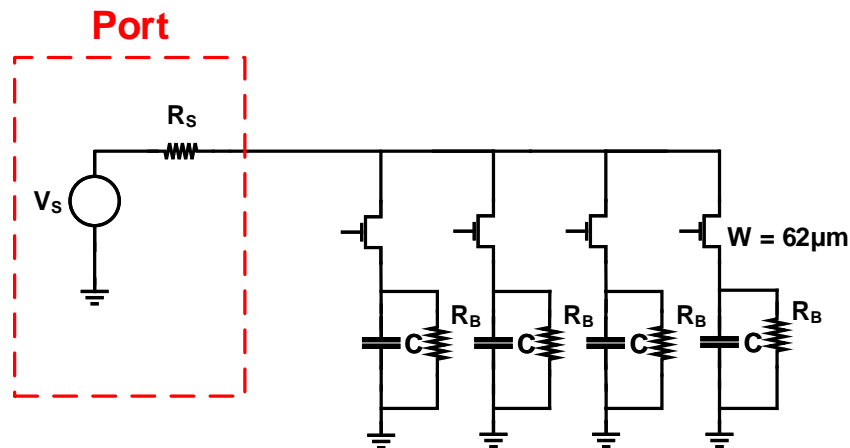


Figure 3.12: Simulation Setup.

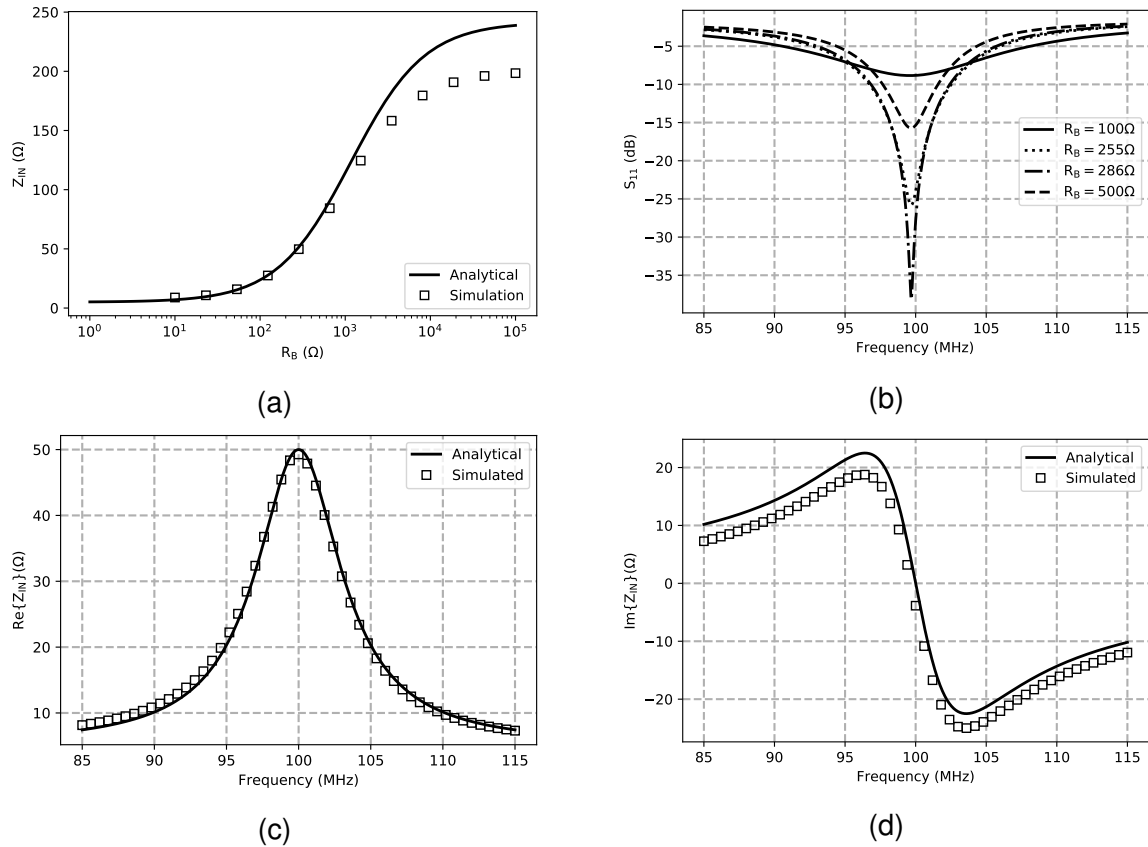


Figure 3.13: (a) Real Part of Z_{IN} versus R_B , (b) S_{11} of the circuit versus the R_B from 85 MHz to 115 MHz, real part of Z_{IN} in function for $R_B = 286 \Omega$, imaginary part of Z_{IN} in function for $R_B = 286 \Omega$

The simulation results demonstrate that the LTI model works correctly with only minor error for high values of R_B . The equation (3.17) correctly characterizes the behaviour of the circuit and to values of R_B close to the ones given by equation (3.18) the impedance matching is ensured (for example for R_B 255 and 286 Ω).

3.5 Conclusion

To sum-up, N-Path circuits are a fairly old concept which has not drawn much attention in the past because of technological limitations. However, with the evolution of CMOS nodes, N-Path circuit have been an important theme in recent years research because they enable a good integration, reconfigurability, high-Q filters and also enables mixer-first receivers. The result of this research addressed already high end models (DARVISHI, ; ANDREWS; MOLNAR, 2010; GHAFARI et al., 2011;

MIRZAEI; DARABI; MURPHY, 2012; IIZUKA; ABIDI, 2016a, 2016b; IIZUKA; ABIDI, 2016b) allowing first cut design. Furthermore, it gives the important trade-offs of such circuits (number of phases, size of switches, etc) (GHAFARI et al., 2011; XU; ZHU; KINGET, 2014). However there is still the technological barrier for higher frequency non-overlapping clocks and thus the center frequency of the filter. Then, non-zero ON switch impedance R_{SW} which limits the maximum rejection of the filter and increases its insertion loss (equations (3.10) and (3.9)). Finally, generally the filter is placed after the antenna, thus the impedance seen by the filter R_S is close to 50Ω , requiring the capacitance of each path to be large for small channel selection.

Two solutions for the resistances limitations can be implemented for channel selection filters, using a wideband LNA. By putting an N-Path BPF after a wideband LNA, the input impedance R_S seen by the N-Path filter can be increased (see figure 3.14a), this would relax both the size of the capacitance of each path and the insertion loss of the filter (KLUMPERINK; WESTERVELD; NAUTA, 2017; XU; ZHU; KINGET, 2014). Another solution is to place an N-Path Notch Filter in parallel to an LNA (see figure 3.14b), by doing this the N-Path Filter would benefit from the Miller effect relaxing both R_{SW} and capacitance size constraints (PARK; RAZAVI, 2014).

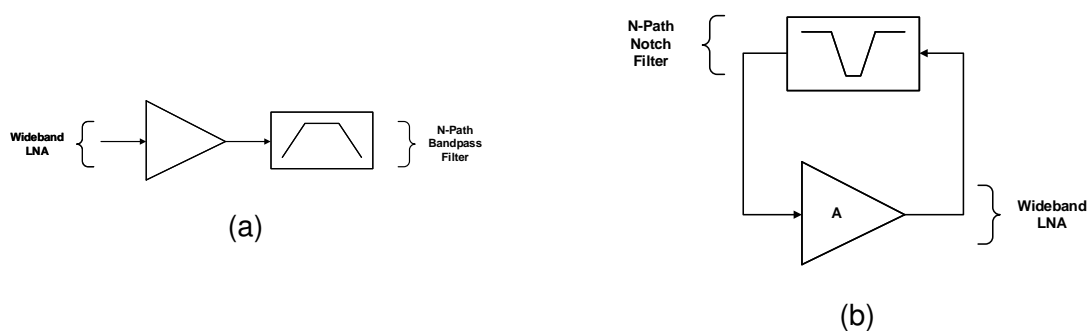


Figure 3.14: Wideband LNA with: (a) series BPF, (b) parallel notch filter.

CHAPTER 4

BAND SELECTION USING N-PATH FILTERS

N-Path circuits are interesting to address a great deal of requirements in Rx. Mixer-first topologies can be used to save power and increase linearity at the cost of NF requirements (ANDREWS, 2012; KLUMPERINK; WESTERVELD; NAUTA, 2017; YANG; YÜKSEL; MOLNAR, 2015; ANDREWS; MOLNAR, 2010; ANDREWS et al., 2012; YANG; ANDREWS; MOLNAR, 2015). N-Path Notch filters can suppress blockers with moderate non-linearities and insertion losses (GHAFARI; KLUMPERINK; NAUTA, 2013). N-Path BPF achieve frequency band selection limited by the frequency, size, and rejection. The size and rejection limitations can be addressed with active circuitry (DARVISHI, ; DARVISHI et al., 2012; DARVISHI; Van Der Zee; NAUTA, 2013) or using LNAs in series (KLUMPERINK; WESTERVELD; NAUTA, 2017; XU; ZHU; KINGET, 2014) or in parallel (PARK; RAZAVI, 2014) (the latter being a Miller Band-pass Filter and not necessarily an N-Path BPF), at the cost of power consumption and linearity. In this work, the channel selection using N-Path filter is studied. This chapter illustrates the performances of different types of BPF filters and presents a Miller Bandpass Filter (MBPF) using the LNA from (De Souza; MARIANO; TARIS, 2017). While (PARK; RAZAVI, 2014) already demonstrates the benefits of an MBPF, in this work, thanks to the proposed LNA, better performances can be expected, especially for the linearity and power consumption. In the first part of this chapter, the proposed LNA is described, then the BPF and finally the MBPF.

4.1 Low Noise Amplifier

The LNA proposed here has been presented in (De Souza; MARIANO; TARIS, 2017). The goal of this original work is to create a generic, inductorless and wideband LNA, that could be digitally tuned. Its schematic is presented in figure 4.1a. The main

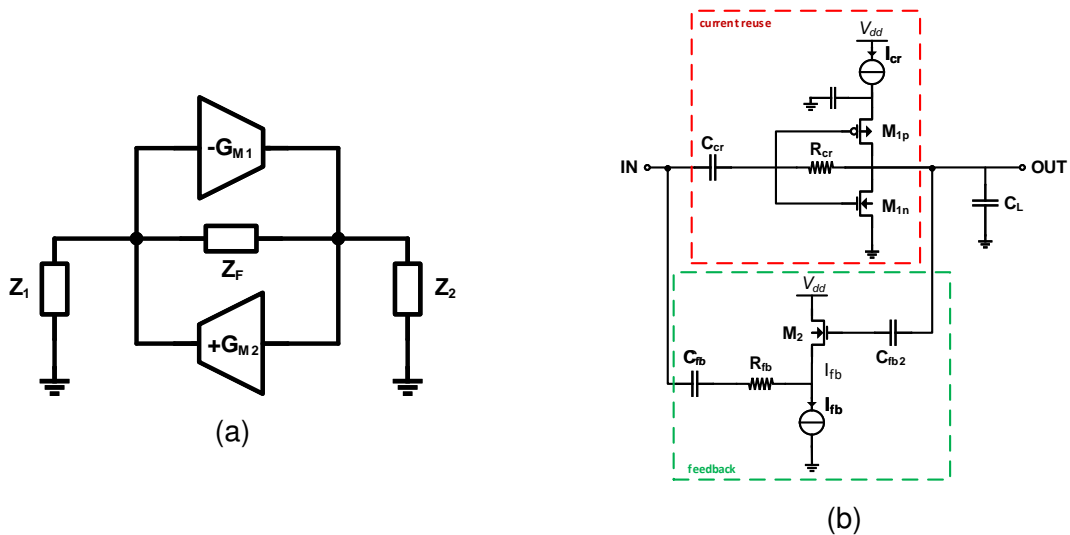
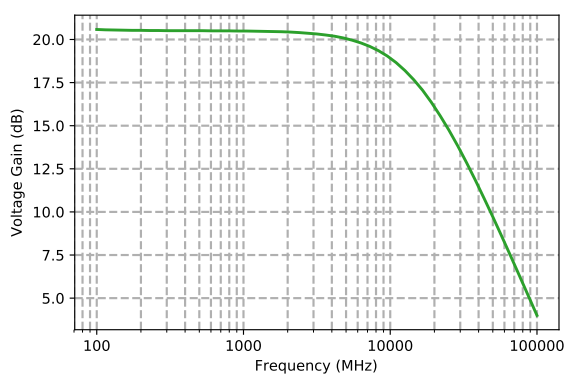
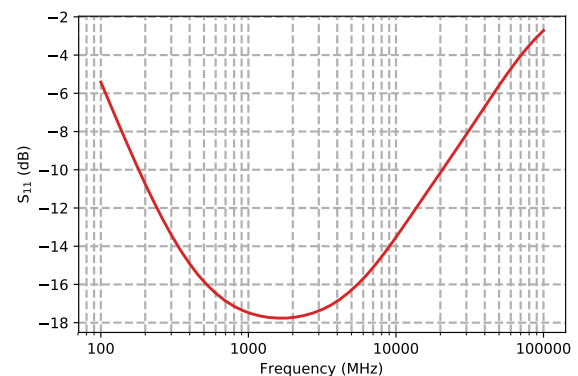


Figure 4.1: (a) Practical gyrator model, (b) LNA implementation.

stage is a current reuse, which achieves a large gain-bandwidth product and a low NF at a moderate power consumption. The active feedback ensures a wideband input impedance matching and a cancellation of inter-modulation. This LNA's equivalent model is presented in figure 4.1b. Here, it is implemented in 28 nm FD-SOI technology. Its gain, input matching, noise figure and linearity response are illustrated in figure 4.2. It presents a voltage gain of 20.5 dB, a S_{11} of -18 dB and a NF of 2.5 dB. The IIP₃ peaks at +8 dBm for nominal operation of the feedback path. The circuit has a bandwidth of 8 GHz (from 300 MHz to 8.3 GHz) in schematic simulation.



(a)



(b)

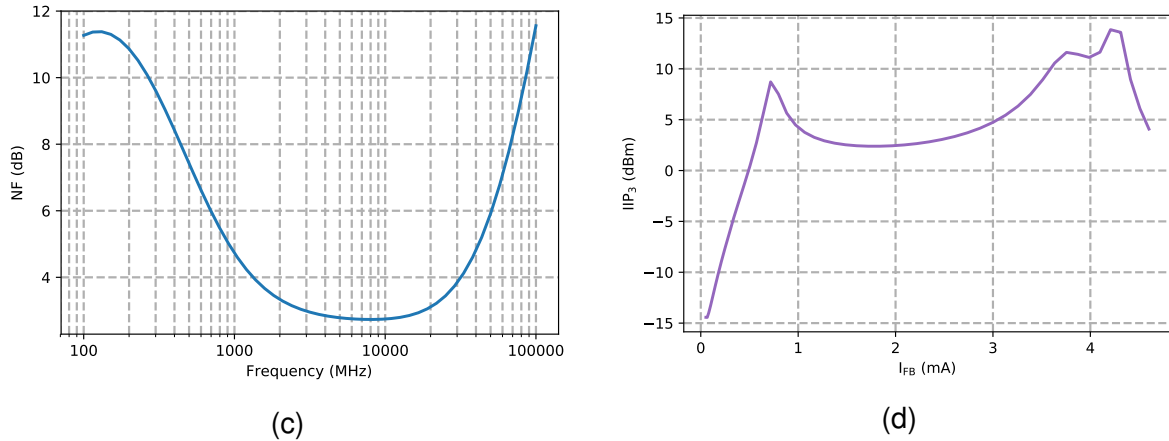


Figure 4.2: (a) Voltage gain, (b) S_{11} , (c) NF, linearity in function of I_{FB} of the base LNA.

Table 4.1: Simulation parameters for the N-Path BPF

Simulation	BW_{-3dB} (MHz)	f_{CLK} (GHz)	R_{SW} (Ω)	R_S (Ω)	N
Single Different Ns	20	1 GHz	5 and 10	50 and 250	4 and 8
Single Two switches	20	1 GHz	5 and 10	50	4 and 8
Differential Two Switches	20	1 GHz	5 and 10	50	4 and 8

4.2 N-Path band-pass Filters

Various configuration of a N-path BPF were explored. First, different on the number of paths is studied, by using equations (3.11-3.13) and then the difference between the usage of one or two set of switches is studied based on figure 4.3a. The advantage of adding a second set of switches is to virtually transform the switch ON resistance to a zero thus increasing the rejection of the filter. Then, the difference between a differential N-Path BPF and a single ended is explored to cancel the even harmonics (see figure 4.3b). Lastly, the behaviour of a higher R_S is simulated to emulate a LNA in series with a N-Path BPF. All the simulations are first performed using perfect switches and no base band resistance (R_B). The parameters selected for these simulations are presented in table 4.1. These circuits are simulated without impedance matching for matters of simplicity, however equation (3.18) could be used to find a R_B which ensures impedance matching.

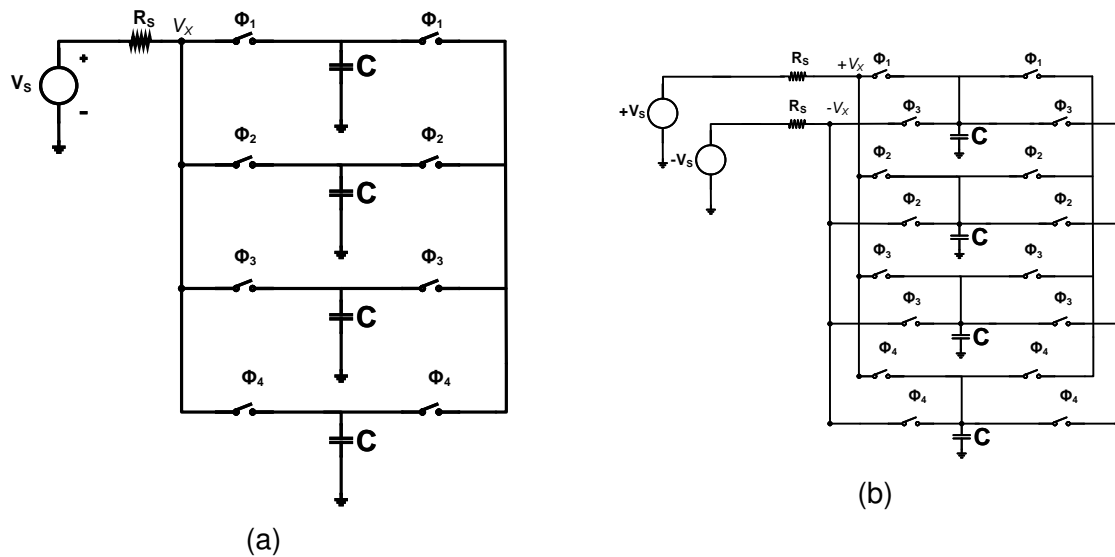


Figure 4.3: (a) 4-Path BPF using two switches, (b) Differential 4-Path BPF using two switches.

The simulation setup is illustrated in figure 4.4. SpectreRF was used as simulator and its PSS, PAC, PSP and PNOISE were explored. The circuit needs a buffer that doesn't affect the impedance presented by the circuit nor by the port to simulate noise, thus a voltage controlled voltage source (VCVS) was used. The noise result for the ideal case is not illustrated because all the noise comes from the harmonics generated and, for an 8-Path filter, those results make little sense to be shown.

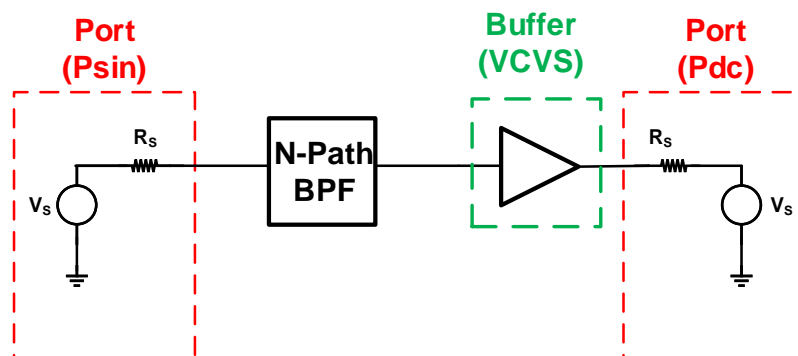


Figure 4.4: Setup used for the simulation of the N-Path BPF

The difference between the harmonic response of a 4-Path and an 8-Path, including the variation of the switch ON resistance R_{SW} , is verified. There are two

important points illustrated in figure 4.5: 1) the harmonic rejection HA higher for a smaller number of paths as predicted by equation (3.11) and 2) by decreasing the switch ON resistance, the total rejection increases by 5 dB as depicted by equation (3.10). This results are shown in table 4.2. To ensure a BW_{-3dB} of 20 MHz, $N \cdot C$ should be equal to 320 pF. The main difference from the number of paths is that with a smaller path the HA decreases, while for a higher number of paths the insertion loss decreases. The first can be calculated by equation (3.11), while the second comes from the nature of the filter. A higher amount of paths enables the output voltage of the filter to be close to a perfect sine.

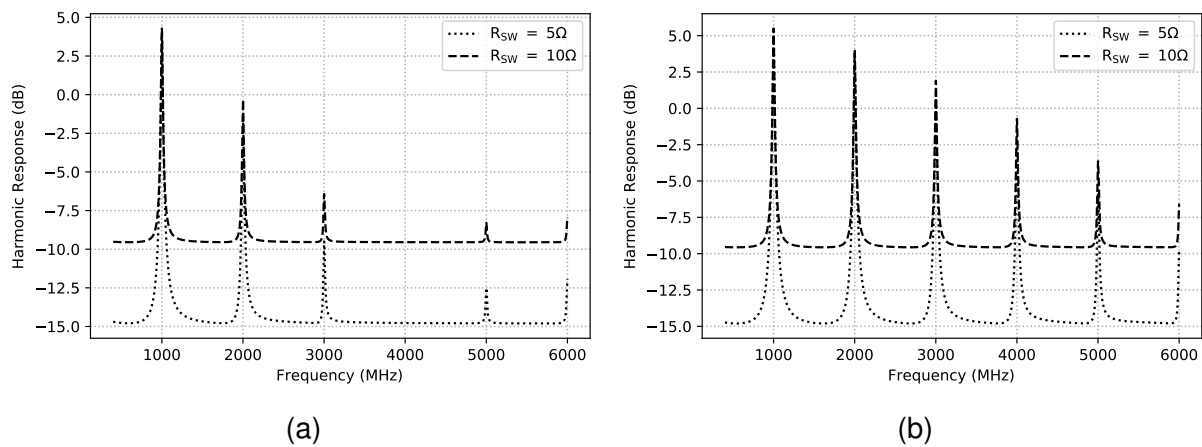


Figure 4.5: Harmonic reponse of: (a) 4-Path BPF with different R_{SW} , (b) 8-Path BPF with different R_{SW} .

Table 4.2: Comparative between number of paths and R_{SW}

		Harmonic Rejection (HA_2 , dB)		Filter Rejection (dB)	
		Simulation	Analytical	Simulation	Analytical
N=4	$R_{SW} = 5 \Omega$	5.4	6.021	19	20.828
	$R_{SW} = 10 \Omega$	4.6	6.021	14.3	15.563
N=8	$R_{SW} = 5 \Omega$	1.9	1.375	19.7	20.828
	$R_{SW} = 10 \Omega$	1.5	1.375	14.9	15.563

Now the same simulation is realized using two switches as depicted in figure 4.3a. By doing this the filter should present a virtual resistance close to zero, increasing largely its rejection while the HA_2 increases slightly (see figure 4.6). The switch resistance, now, has a negligible effect on the rejection of the filter (0.3 and 1.1 dB for already large rejection values). The rejection peaks are not considered in the

filter rejection because they represent a small frequency bandwidth. The higher HA comes from the fact that part of the harmonics is rejected.

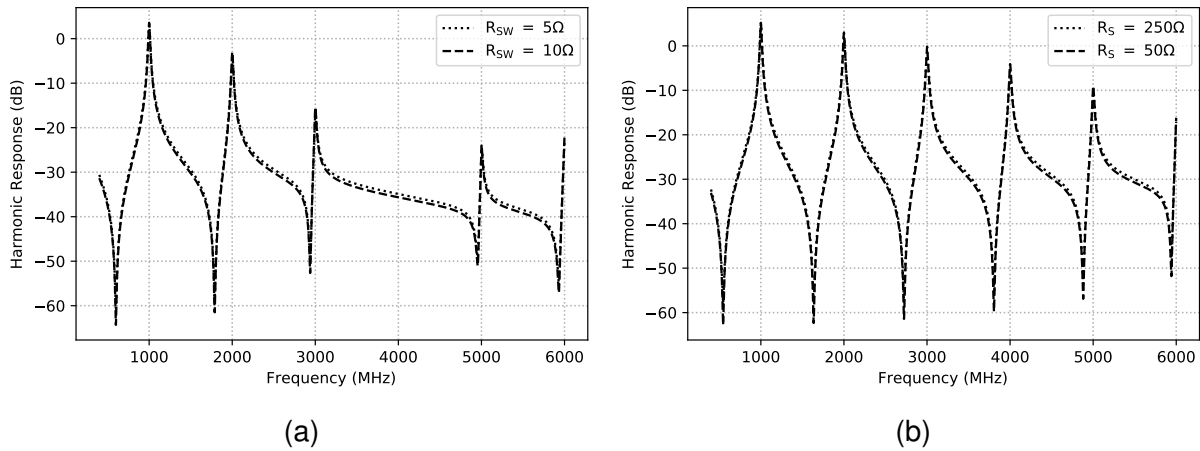


Figure 4.6: Harmonic reponse of: (a) 4-Path BPF with different R_{SW} using two switches, (b) 8-Path BPF with different R_{SW} using two switches.

Table 4.3: Comparative between number of paths and R_{SW} with two switches

		Harmonic Rejection (HA_2 , dB)		Filter Rejection (dB)	
		Simulation	Analytical	Simulation	Analytical
N=4	$R_{SW} = 5 \Omega$	7.1	6.021	33.3	NA
	$R_{SW} = 10 \Omega$	6.6	6.021	33.6	NA
N=8	$R_{SW} = 5 \Omega$	2.8	1.375	35	NA
	$R_{SW} = 10 \Omega$	2.2	1.375	36.1	NA

Because of the effect of a double switch, the simulation to emulate the LNA in series with the N-Path BPF uses only one switch, thus making possible to verify well the effect of a higher R_S . In this case the R_{SW} is set to 5Ω . The rejection and the HA increases, the first not accordingly to the analytic equation. This comes from the fact that both equations (3.10 - 3.11) are approximations of the behaviour of the circuit. This approximations can give a starting point for the design of the N-Path BPF, but margins should be taken into account. The $N \cdot C$ product can be also be divided by five, to 64 pF.

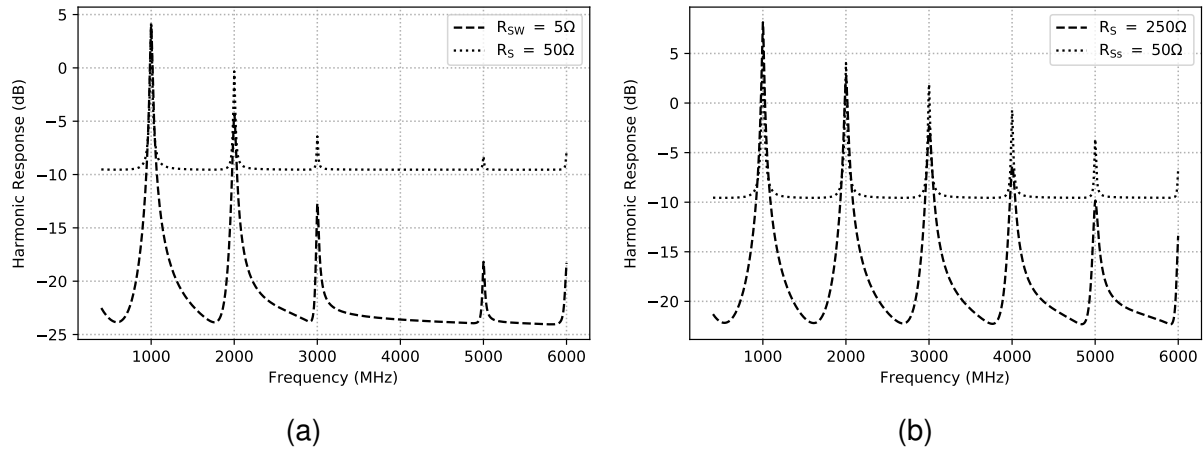


Figure 4.7: Harmonic reponse of: (a) 4-Path BPF with different R_S using one switch, (b) 8-Path BPF with different R_S using one switch.

Table 4.4: Comparative between source resistance, with $R_{SW} = 5 \Omega$

		Harmonic Rejection (HA_2 , dB)		Filter Rejection (dB)	
		Simulation	Analytical	Simulation	Analytical
N = 4	$R_S = 50 \Omega$	5.4	6.021	19	20.828
	$R_S = 250 \Omega$	8	6.021	28	34.151
N = 8	$R_S = 50 \Omega$	1.9	1.375	19.7	20.828
	$R_S = 250 \Omega$	5.5	1.375	30.3	34.151

Lastly the differential filter as depicted in figure 4.3b was simulated, using double switch. By doing this, the even harmonics are cancelled and naturally the 3rd harmonic is the first one that can be seen (see figure 4.8), thus the HA_3 is presented. The filter rejection increases because, by cancelling the even harmonics, the filter keeps following its natural rejection by decade without any peak of gain at those frequencies. We can now see that the filter rejection increases by 10 dB, as presented in table 4.5.

Table 4.5: Results from differential N-Path BPF, with double switch and different R_{SW}

		Harmonic Rejection (HA_3 , dB)		Filter Rejection (dB)	
		Simulation	Analytical	Simulation	Analytical
N=4	$R_{SW} = 5 \Omega$	19	19.085	44.6	20.828
	$R_{SW} = 10 \Omega$	19	19.085	45.7	15.563
N=8	$R_{SW} = 5 \Omega$	6.5	3.774	43.6	20.828
	$R_{SW} = 10 \Omega$	5.4	3.774	45.8	15.563

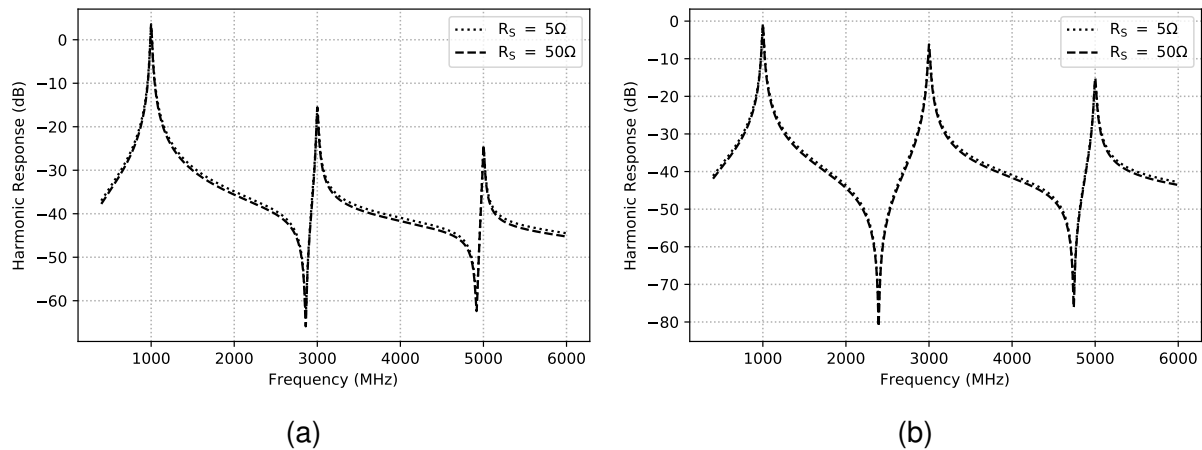


Figure 4.8: Harmonic response of: (a) 4-Path Differential BPF with different R_{SW} using two switches, (b) 8-Path Differential BPF with different R_{SW} using two switches.

N-Path filters become even more interesting with the evolution of CMOS technology, because of its highly linear oxide-capacitors, while - by following Moore's law - it also offers faster digital circuits and better switches in terms of low on-resistance and parasitic capacitances (KLUMPERINK; WESTERVELD; NAUTA, 2017). The transition from an ideal switch to a CMOS switch is relatively small with the 28 nm FD-SOI technology. To confirm this behaviour two N-Path BPF are simulated, with a $R_{SW} \approx 5\Omega$, only one switch, 4 and 8 paths (see figure 4.9) and at $f_{CLK} = 1\text{ GHz}$. The difference in the rejection is about 2 dB, for both cases. The in-band gain decreases by 0.3 to 0.4 dB, while the rejection floor decreases from 1.5 to 1.7 dB. While there are parasitics that are added, it is important to note that the switch on-resistance is actually higher than 5Ω and this has an influence in the presented results.

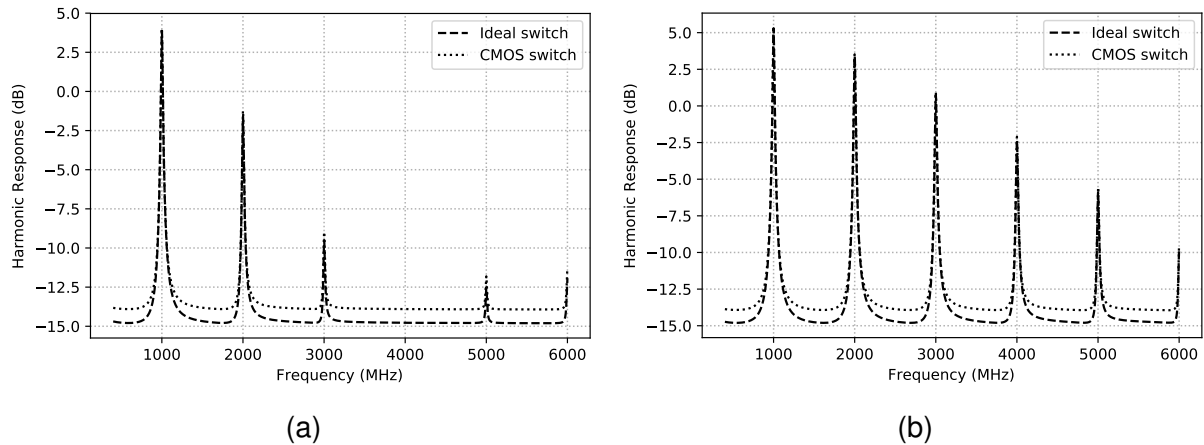


Figure 4.9: Comparison of harmonic response of: (a) a 4-Path BPF real and ideal, (b) an 8-Path BPF real and ideal.

The impedance matching is simulated by adding a resistor R_B equal to 276 and 424 Ω (for 4 and 8-Path, respectively) calculated with equation (3.18) (see figure 4.10). It is possible to see the S_{11} present values close to 0 dB without matching, while with matching it presents very good matching at $S_{11} < -30$ dB. Lastly, the NF of both the real BPF non-matched and matched is compared (see figure 4.11). Since the N-Path BPF consists of capacitances and CMOS switches only, its NF is relatively low at 0.7 dB for the worst response. Considering the matched circuit, the resistance is responsible for the majority of the noise, increasing the NF to 2.5 to 3 dB. It also degrades the gain of the circuit by 2 to 3 dB (see figure 4.12).

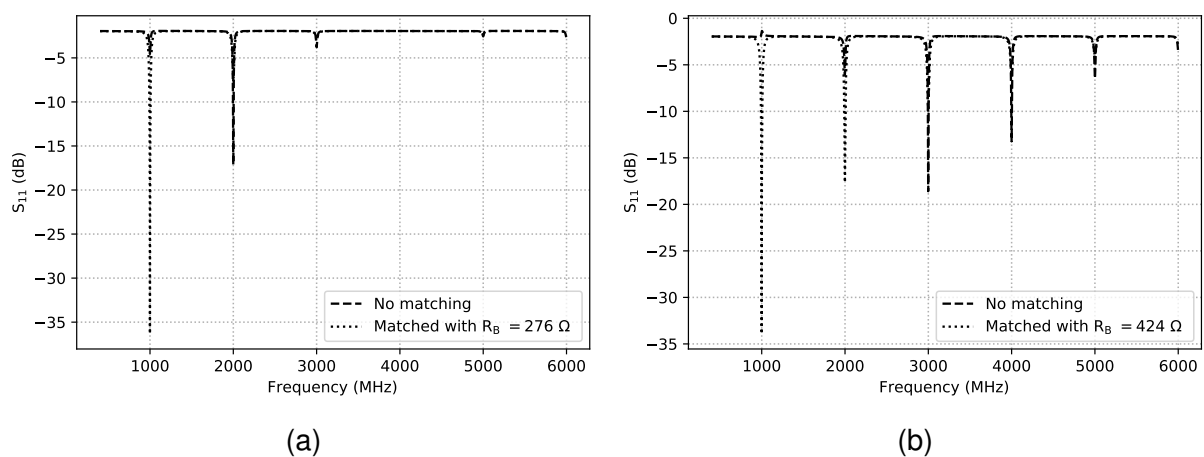


Figure 4.10: Comparison of S_{11} of: (a) a 4-Path BPF, (b) an 8-Path BPF.

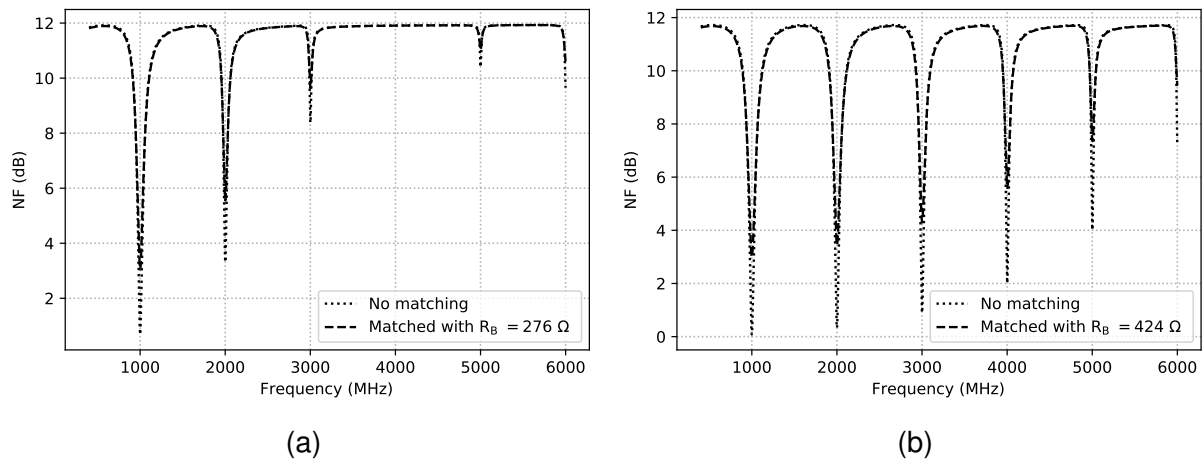


Figure 4.11: Comparison of NF of: (a) a 4-Path BPF, (b) an 8-Path BPF.

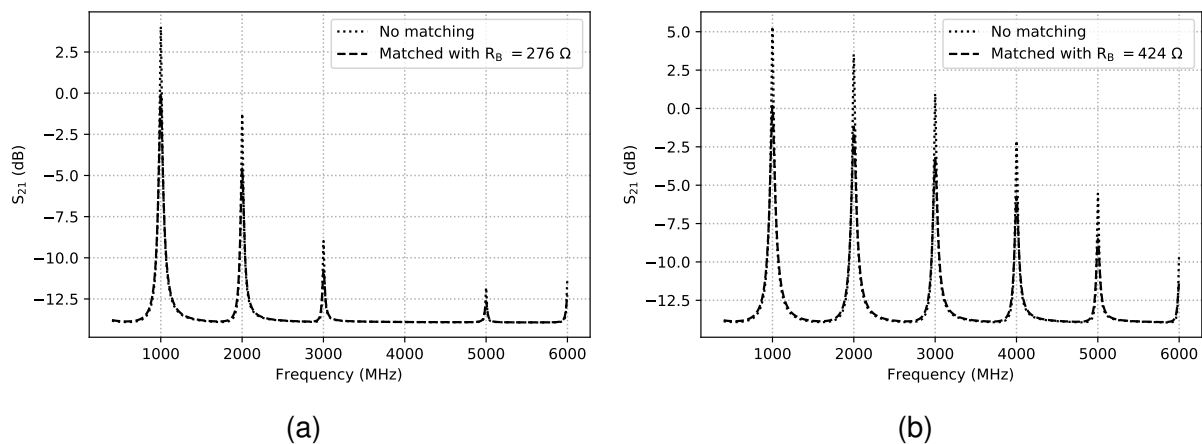


Figure 4.12: Comparison of harmonic response of: (a) a 4-Path BPF real, (b) an 8-Path BPF.

As illustrated, the transition from the ideal switch to the CMOS switch does not change the harmonic response of the filter, it only lead to a difference between 1.5 and 1.7 dB in the rejection and 0.4 dB in the insertion loss. However the filter by itself is not matched, which would also be the case for the ideal switches. One solution is to match the source impedance for the filter, this requires the filter to be simulated and then the source impedance to be matched such as in (GHAFFARI et al., 2011; GHAFFARI; KLUMPERINK; NAUTA, 2010, 2013; GHAFFARI; KLUMPERINK; NAUTA, 2013). However, the impedance matching using equation (3.18) creates a simple and accurate model to match our filter to a given source, the drawback is that this increases the NF (about 2 dB) while creating a bigger insertion loss and thus decreasing the rejection by the same value (between 2 and 3 dB in the simulated cases).

4.3 Miller Bandpass Filter

The implementation of a MBPF is interesting to reduce the size of the required capacitors and to ensure channel selection. This has been presented in (PARK; RAZAVI, 2014), with the circuit depicted in figure 4.13. A wideband LNA is used with an N-Path notch filter as feedback loop. The circuit behaves as follows: in the reject band of the notch filter, it presents a very high impedance, thus the signal goes mainly through the LNA. Out of the reject band, the notch filter presents a moderate impedance, and the parallel product between LNA and filter is naturally mismatched to the source impedance, thus rejecting the input signal. Additionally, the filter sees an amplification of the source impedance of $(1+A)$ times, A being the gain of the LNA, due to the Miller effect, while the source sees the equivalent capacitance given by:

$$C_{EQ} = \frac{NC}{(1 + A)}. \quad (4.1)$$

The filter should also add little noise to the LNA. The main drawback observed in (PARK; RAZAVI, 2014) is the in-band linearity. By adding the LNA from (De Souza; MARIANO; TARIS, 2017), the linearity can be improved while maintaining the same performances (NF and voltage gain) for a similar or even lower power consumption.

There are some questions that urge from this LNA compared to the LNA from (PARK; RAZAVI, 2014). Firstly the impedance seen by the N-Path notch filter from (PARK; RAZAVI, 2014) is the source impedance in parallel to a virtual ground, thus making the impedance R_S seen by the filter to be equal to 50Ω while our LNA has a wideband impedance matching, presenting always 50Ω at the input and thus making the impedance R_S seen by the notch filter to be equal to 25Ω . Then the feedback from the presented LNA uses the non-linearities of the signal to cancel the 3rd order products, while (PARK; RAZAVI, 2014) uses a simple resistive feedback. Lastly, this LNA is more sensitive to capacitive charges at the output than the work in (PARK; RAZAVI, 2014). However the standard equations from (PARK; RAZAVI, 2014) can be used to describe the -3 dB bandwidth and filter rejection of the proposed

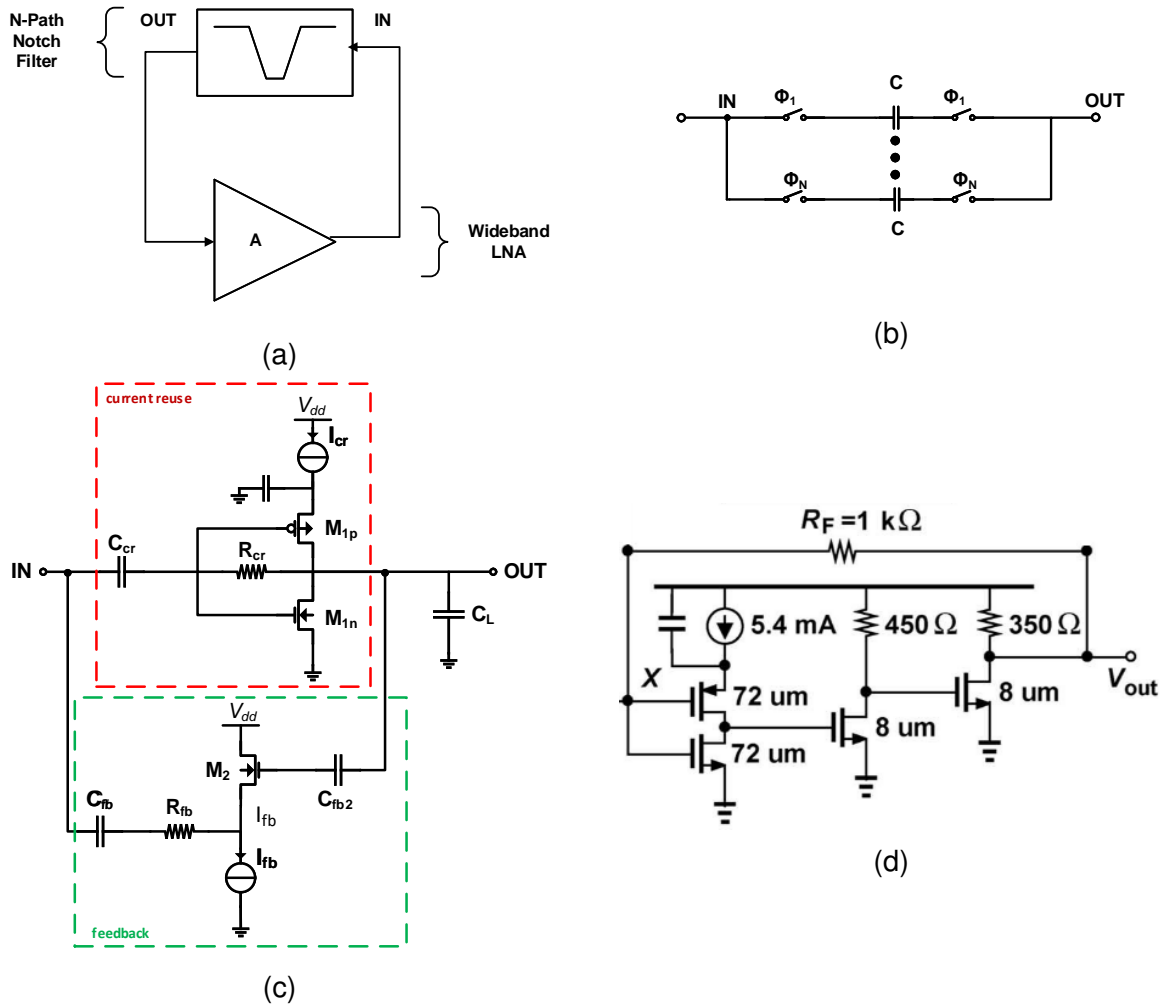


Figure 4.13: (a) Miller Bandpass filter, (b) N-Path notch filter implementation, (c) LNA from [1], LNA from [7].

implementation, given by:

$$BW_{-3\text{db,MBPF}} = \frac{1}{2\pi N R_S C (1 + A)}, \quad (4.2)$$

$$\text{Rejection}_{\text{MBPF}} = \frac{\frac{R_{\text{SW}}}{(1+A)}}{\frac{R_{\text{SW}}}{(1+A)} + R_S} = \frac{R_{\text{SW}}}{(1 + A)R_S + R_{\text{SW}}}, \quad (4.3)$$

where A is the voltage gain of the LNA, R_S the source resistance, R_{SW} the switch resistance. The product $N \cdot C$ is now divided by $(1+A)$. The gain of our LNA is 20 dB. This should reduce the product $N \cdot C$ to 32 pF for a 20 MHz bandwidth in contrast to the 320 pF required for a simple N-Path BPF or the 64 pF for a 250 Ω source resistance. However, because the source impedance becomes $\approx 25 \text{ }\Omega$, the $N \cdot C$ stays at 64 pF.

To relax the design constraints and have a margin for the post-layout simulations, the final $N \cdot C$ product chosen is 80 pF. The circuit was simulated for the cases presented in table 4.6 using ideal switches.

Table 4.6: Simulation parameters for the MBPF

Simulation	BW_{-3dB} (MHz)	f_{CLK}	R_{SW} (Ω)	R_S (Ω)	N
Single	20	2 GHz	5 and 10	50	4 and 8
Pseudo-differential	20	2 GHz	5 and 10	50	4 and 8

The pseudo-differential is obtained by simply putting two LNAs at the output of the source (see figure 4.14). Some hypotheses can be made beforehand: 1) by increasing the number of paths the noise figure should be smaller while the in-band gain should be higher, 2) the spectrum of the 4-Path filters should be cleaner and present lower HAs, 3) the noise figure of the differential circuit should be smaller because of the cancellation of the even harmonics. The simulation results are presented in figures 4.15 and 4.16.

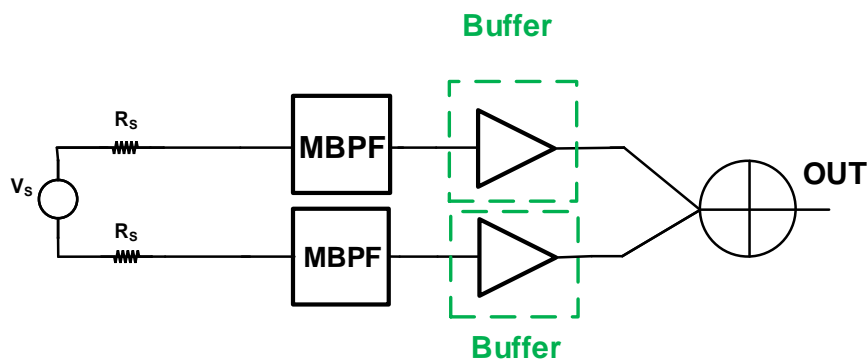


Figure 4.14: Pseudo-differential circuit.

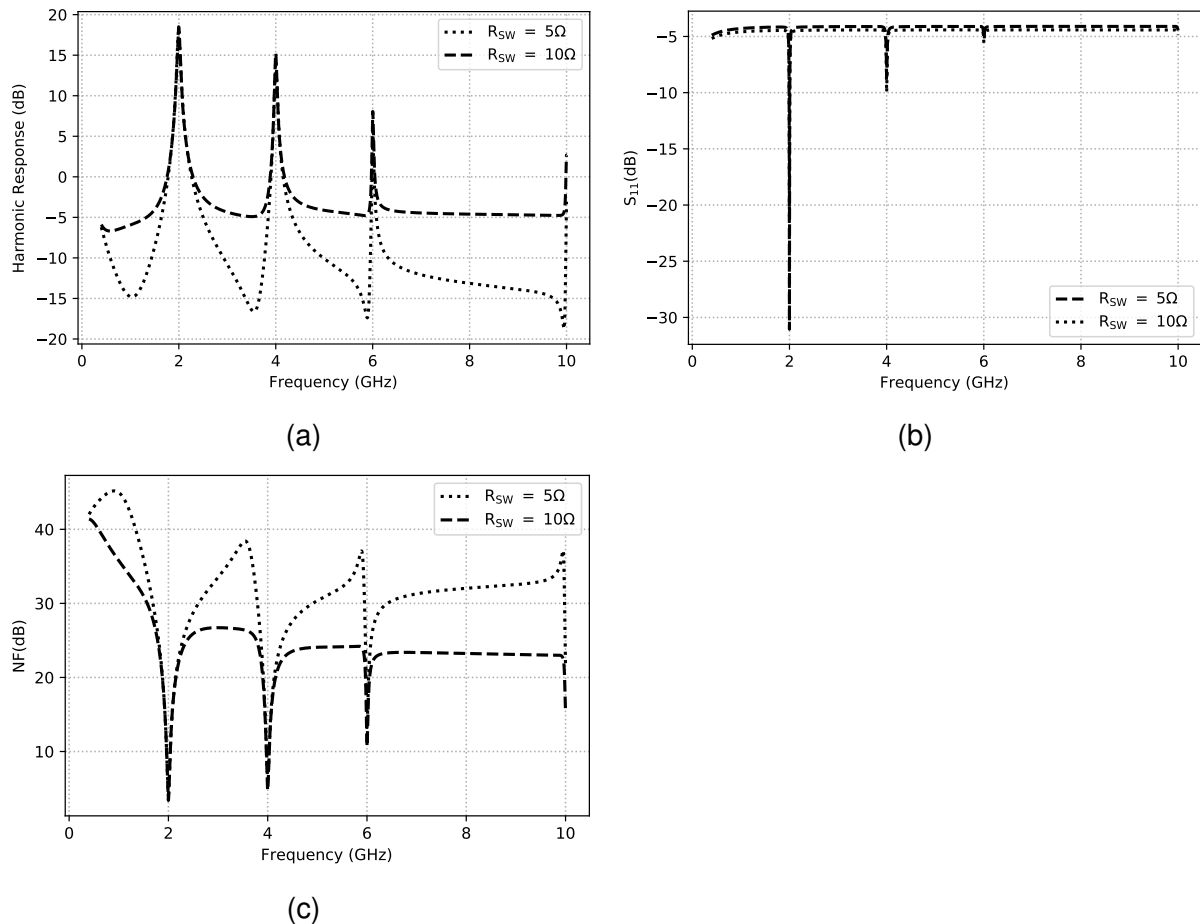


Figure 4.15: Simulation results of a 4-Path single ended MBPF: (a) Harmonic Response), (b) S_{11} , (c) NF

As expected, by increasing the number of paths the maximal in-band gain increases slightly and the NF decreases. The in-band gain difference between the 4 and 8 path is 0.6 db (18.5 dB for the 4 path and 19.1 dB for 8 path). The NF difference can be from 0.3 to 0.5 dB depending on the switch on-resistance. Now it is necessary to verify if the pseudo-differential circuit decreases the noise contribution of the harmonics. Figures 4.17 and 4.18 present the results. As predicted, the pseudo-differential circuit reduces the noise, however this reduction is very small (0.1 dB), while not changing the in-band gain. A comparative table is presented in table 4.7. By increasing the switch impedance, the NF of the circuit decreases (this is more evident for the 4-Path) for all of the cases at the cost of the filter rejection. The circuit is always matched due the impedance presented by the notch filter is very high and the parallel between the impedances of the notch filter and the LNA end up being

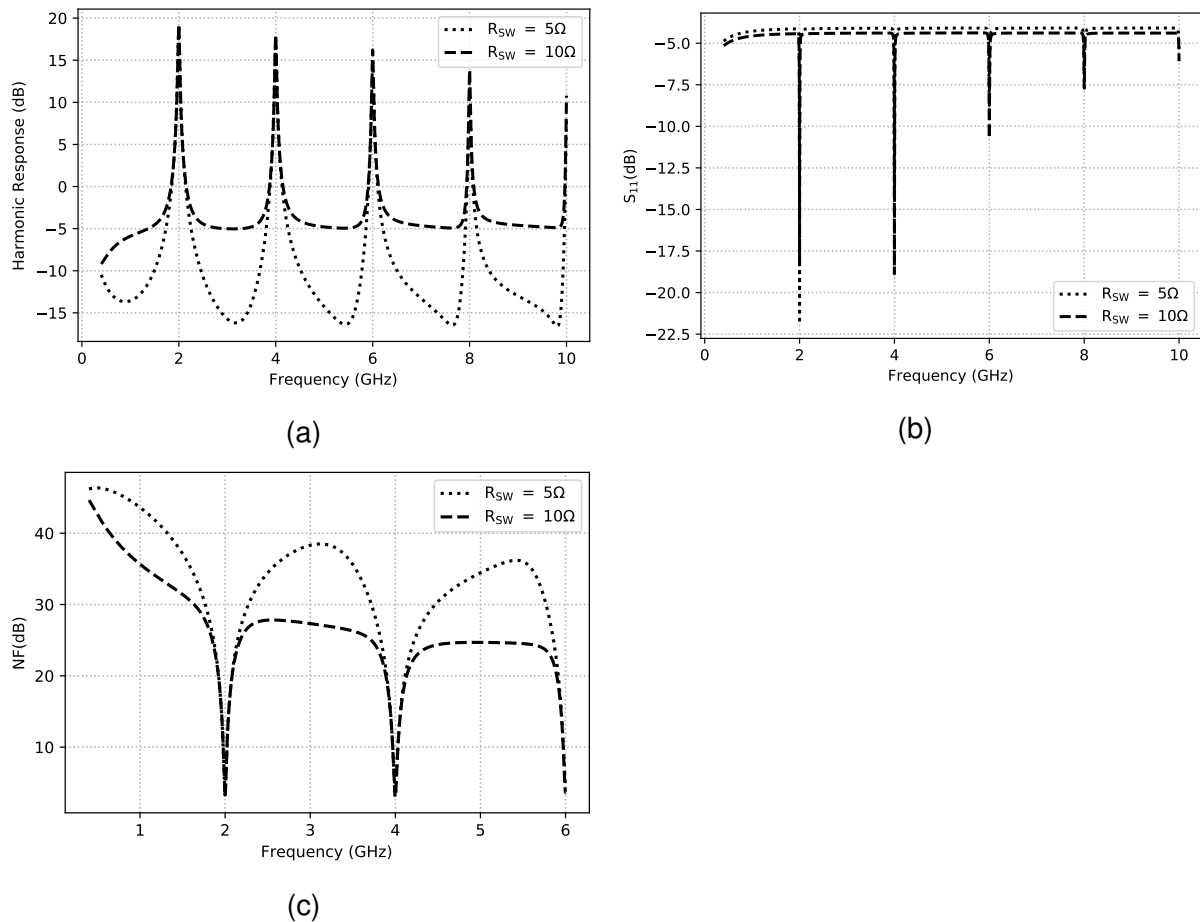
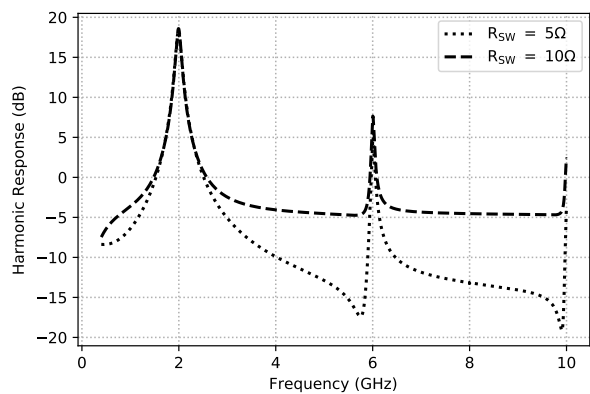


Figure 4.16: Simulation results of an 8-Path single ended MBPF: (a) Harmonic Response, (b) S_{11} , (c) NF

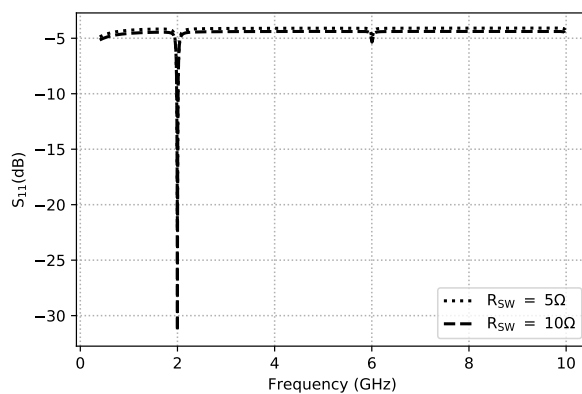
approximately equal to the LNA impedance, which is always matched to 50Ω . Furthermore, with the pseudo-differential circuit, the consumption of the LNA core doubles and the consumption of the non-overlapping clocks increases by at least 20%.

Table 4.7: Comparative between all the simulated circuits

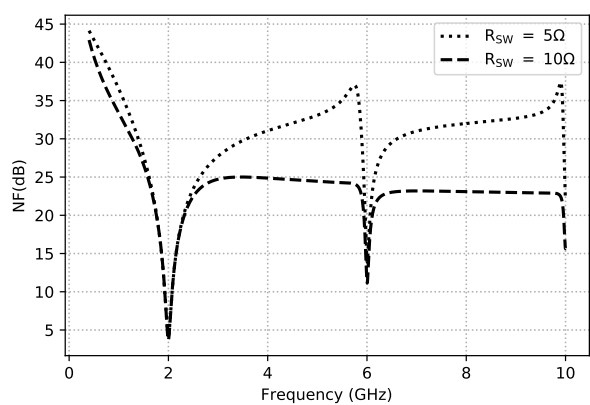
			NF (dB)	S_{11}	Rejection (dB)	HA_2	HA_3
Single ended	N = 4	$R_{SW} = 5\Omega$	3.7	-33	37	4	NA
		$R_{SW} = 10\Omega$	3.4	-21	22.9	3.3	NA
	N = 8	$R_{SW} = 5\Omega$	2.9	-21	35.7	1.6	NA
		$R_{SW} = 10\Omega$	2.8	-18	24.1	1.3	NA
Differential	N = 4	$R_{SW} = 5\Omega$	3.4	-31	37.4	NA	13.2
		$R_{SW} = 10\Omega$	3.1	-22	22.8	NA	11
	N = 8	$R_{SW} = 5\Omega$	2.8	-19	36	NA	3.6
		$R_{SW} = 10\Omega$	2.7	-17	25.9	NA	2.8



(a)

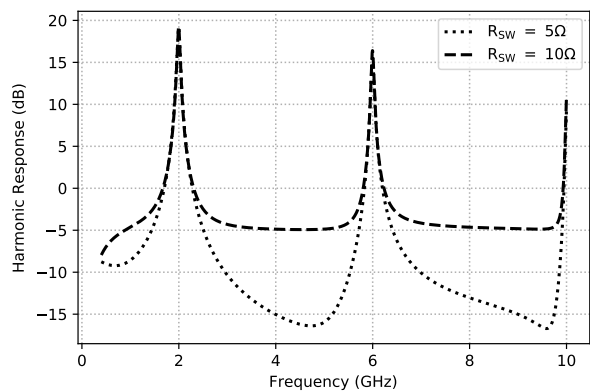


(b)

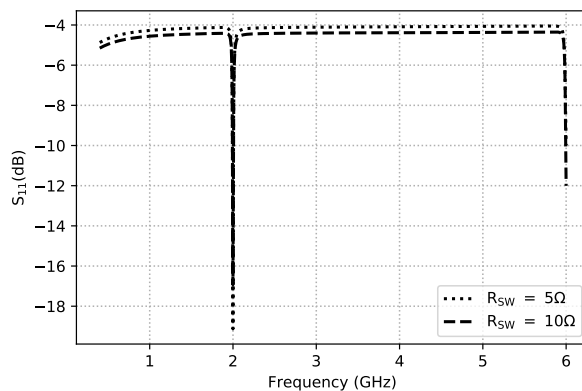


(c)

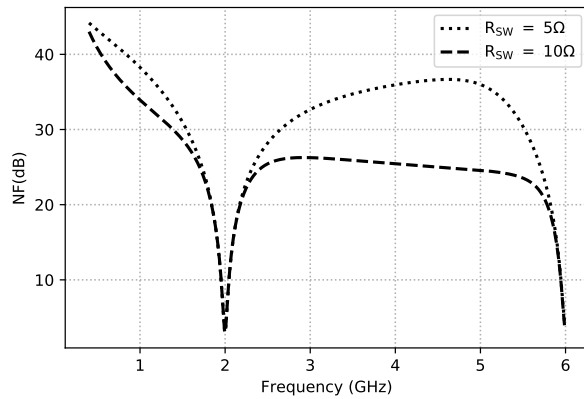
Figure 4.17: Simulation results of a pseudo-differential 4-Path MBPF: (a) Harmonic Response , (b) S_{11} , (c) NF



(a)



(b)



(c)

Figure 4.18: Simulation results of a pseudo-differential 8-Path ended MBPF: (a) Harmonic Response, (b) S_{11} , (c) NF

4.4 MBPF implementation with CMOS switches

The combination of a LNA with a N-path filter in a feedback arrangement requires some specific concerns about the overall behavior of the system. Among them is the impact of the switch parasitics. This can have a large impact in the performance of the circuit due the sensibility of the LNA to capacitive loads. In this part, the final circuit including CMOS switches is sized to ensure the specifications listed in table 4.8.

Table 4.8: Circuit requirements

Frequency	Gain	S_{11}	Power Consumption	NF	BW_{-3dB}
400 MHz - 6GHz	>15 dB	<10 dB	<20 mW	<3.5 dB	20 MHz

4.4.1 Circuit sizing

The clock generation circuit presented in chapter 2 consumes from $700\mu\text{W}$ to 5.7 mW for the frequency range required. This can further be reduced by 20% (about 1 mW for the highest consumption) by adjusting the back-gate of the transistors. Thus the power consumption of the rest of the circuit should not be higher that 15 mW. Because the LNA is the only active circuit, it can consume 15 mW by itself. By using a pseudo-differential or a single-ended N-Path the main improvement is the cancellation of even harmonics, but this comes at an extra power consumption. Because the LNA

circuit already consumes 7 mW, the pseudo-differential topology is not further explored in the proposed implementation. To keep the NF as low as possible, an 8-Path filter is used, this also can relax the gain requirements. By choosing an 8-Path, the insertion loss of the filter is smaller, however the off-capacitance presented by the filter is increased, the trade-off between in-band gain and the number of paths must be discussed. Even further, the switch off-capacitance should reduce the gain-bandwidth (GBW) product, and the bandwidth as well, of the overall LNA. To have the highest rejection, the switch on-resistance is set to 5Ω . If a higher switch on-resistance was chosen, the power consumption of the clock generation circuit could be decreased, but the rejection and in-band gain would also slightly decrease. Finally, the C capacitance and the $N \cdot C$ are kept as the same as for ideal cases (10 pF and 80 pF). This creates a -3dB bandwidth of about 24 MHz, which gives the circuit a margin for layout. The parameters selected for this design are reported in table 4.9.

Table 4.9: Circuit design choices

P_{CLK}	P_{LNA}	N	R_{SW}	C	$N \cdot C$	BW_{-3dB}
700 μ to 5 mW	7 mW	8	5Ω	10 pF	80 pF	24 MHz

For matters of simplicity, the circuit was simulated from 1 to 5 GHz with the clock frequency being spaced by 1 GHz. The presented results cover a band of $f_{CLK} \pm 300$ MHz. Because of the switches off-capacitance, the GBW of the LNA decreases with the increase of the frequency, at 1 GHz the circuit presents a gain of 19 dB, at 5 GHz it is 16.5 dB (see figure 4.19). This has an influence over the rejection that at 1 GHz is 25.6 dB, while at 5 GHz it is 20.5 dB.

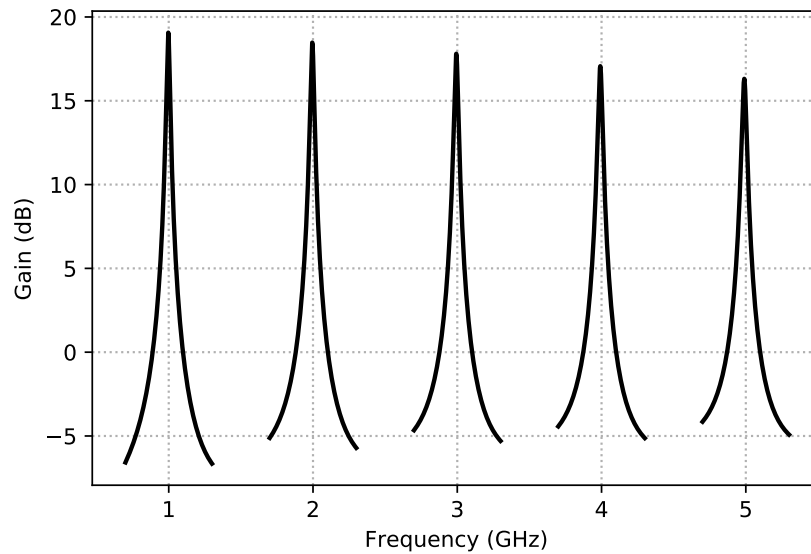


Figure 4.19: Harmonic response of the final circuit

As discussed previously, while in the reject band of the filter, the circuit behaves mainly as the LNA alone. This is verified by figures 4.2 and 4.20. Indeed, the MBPF impedance matching follows exactly the same behaviour as the standalone LNA, but with a smaller bandwidth.

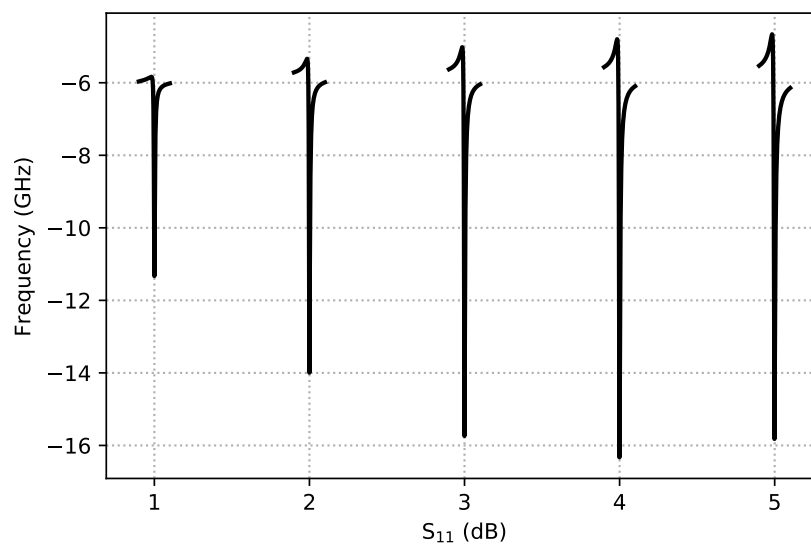


Figure 4.20: S_{11} of the final circuit

Because the influence of the switches off-capacitance, the GBW decreased. This also has an influence over the NF response, it is still 2.9 dB at 4 GHz. (see figure 4.21). Table 4.10 groups all the highest simulation results at a given frequency. The

final consumption of the LNA is 6.5 mW, and the total consumption of the circuit at the highest frequency, 6 GHz, is only 12.2 mW.

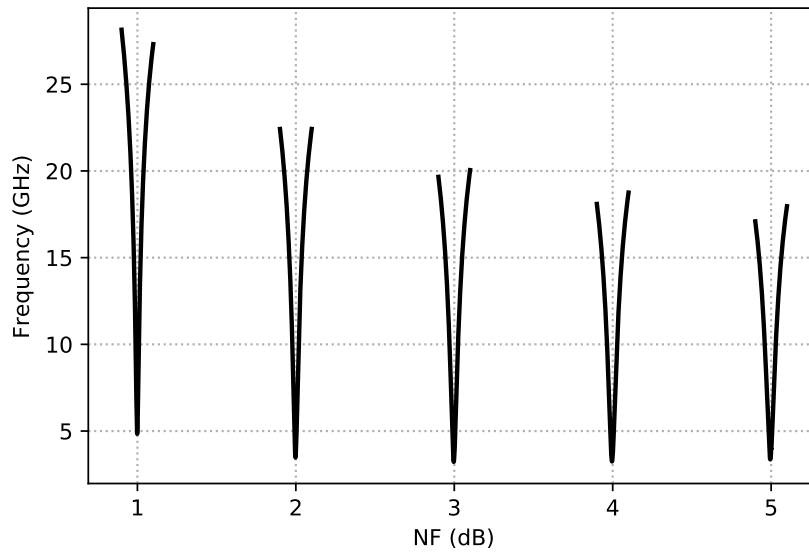


Figure 4.21: NF of the final circuit

Table 4.10: Final circuit simulation results

Gain	Rejection	S_{11}	NF
19 dB @ 1GHz	25.6 dB @1GHz	-16.1@4GHz	2.9 @4GHz

Finally, the linearity of the circuit is simulated using SpectreRF's PSS simulation. The simulation setup is such as the $f_{CLK} = 2$ GHz. The first tone is at a frequency $f_1 = 2$ GHz, the second one is at the frequency $f_2 = f_1 + \Delta_f$, with $\Delta_f = 5$ MHz. The input power for the tones is -40 dBm. A sweep of V_{FB} is done to search the optimal point of linearity, this voltage controls the current of the current mirror used. As expected, the in-band linearity IIP_3 is close to the one from the LNA, having a maximum of 7 dBm (see figure 4.22).

4.5 Layout of the circuit

The beginning of the layout is illustrated in figure 4.23, presenting the Inverter and NAND. The size of this circuit is explained in the appendix A. However, the common transistor used for all this circuit is a 6 μm transistor, with six fingers. Creating a

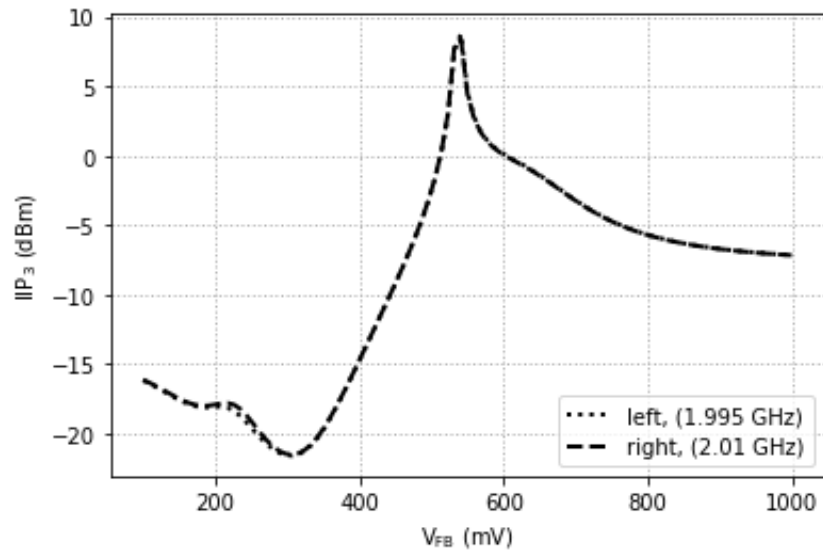


Figure 4.22: IIP₃ versus V_{FB} for the final circuit

multi-finger transistor reduces its parasitics while also helping the arrangement of the final design. Dummies are also added on top of the transistors and at its side, this is required at advanced nodes in order for the fabrication process to be more robust.

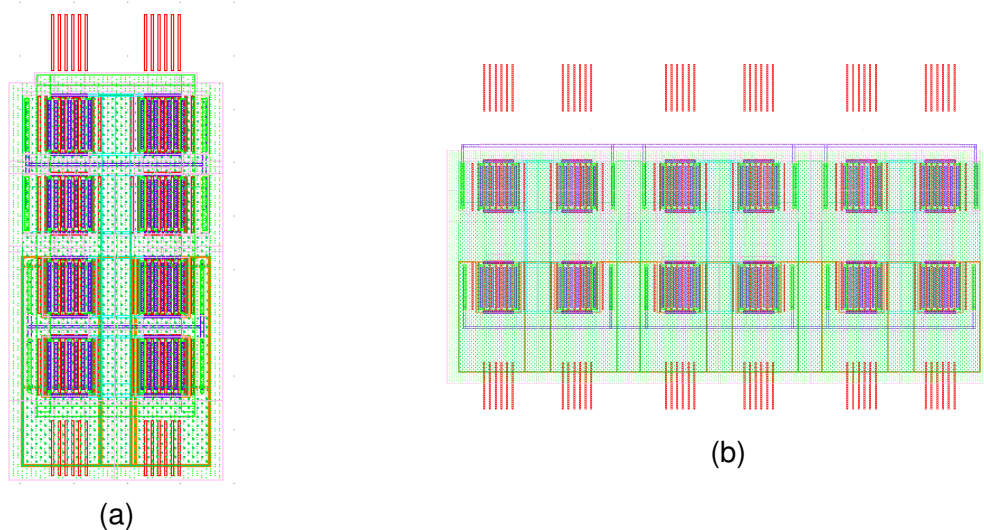


Figure 4.23: Layout of: (a) Inverter, (b) 3-Input Nand.

4.6 Conclusion

N-Path filters enable an efficient reconfigurability. However, simple BPF require large capacitances to properly select a channel, for instance, in this case, 320 pF are

required for 20 MHz and even higher for smaller channels such as the 200 KHz from GSM. To relax the capacitance requirement the input impedance could be increased, by adding a LNA before the filter and the filter can be properly matched using the presented LTI model at the cost of the global gain of the circuit. The MBPF emerges as another good option to reduce the size of the required capacitance by $(1+A)$, only if the LNA has a high impedance at its input. Even more, the designs can be optimized by using a differential antenna and a differential N-Path (with a pseudo-differential or differential LNA for the MBPF), cancelling the even harmonics. However this comes at the cost of power consumption that increases for both non-overlapping clocks generation and LNA. While not being a novel circuit, N-Path circuits are still being developed and various solutions to address the different necessities of the circuit are being studied, from its model to the harmonic cancellation. However, the linearity of the circuit is not fully addressed. While there are some circuits that present high out-of-band linearity (KLUMPERINK; WESTERVELD; NAUTA, 2017), no circuit seems to present a high linearity at the in-band of the filter (higher than -10 dBm). The loop LNA and filter proposed here achieve a gain of 19 dB with a rejection 25.6 dB, a low NF of 2.9 GHz while keeping a S_{11} lower than -10 dB at the selected frequency. It also ensures a high in-band linearity of 7 dBm thanks to the local feedback linearization embedded in the proposed LNA configuration. This circuit is compared to the SoA in the last chapter.

CHAPTER 5

CONCLUSION

N-Path circuits are interesting solutions for reconfigurable wideband Rx RFFE. Because of CMOS technology, higher center frequencies can be achieved, thus creating high-Q filters that can be easily integrated with the RFFE. While not a novel solution, the implementation of such circuits was not viable until the CMOS technology achieves transit frequency above 100 GHz. The recent works related to N-Path circuit focus on: modeling harmonic and folding cancellation, reducing capacitance sizing, power consumption (mostly from clock generation) while increasing frequency and even remove the traditional LNA (mixer-first circuits). The present work went through some of the SoA circuits, while analyzing and validating the existing models. Finally, the main interest was to prove the feasibility of band selection with high linearity by unifying the works from (De Souza; MARIANO; TARIS, 2017) and (PARK; RAZAVI, 2014). Due to time constraints, post-layout simulations were not included in this thesis, but the layout is currently being realized. Even without post-layout simulation, this work places itself close to the SoA as illustrated in 5.1. Thanks to the 28 nm FD-SOI, this circuit can address standards up to 5 GHz whereas other works are limited around 2 GHz. The gain is slightly lower but if needed, it can be increased by increasing the current consumption which is half the current consumption of (PARK; RAZAVI, 2014) and (QI et al., 2017). The NF is similar for all the works, around 3 dB. Finally this works offers the highest rejection, 26.5 dB, and the highest in-band linearity with an IIP_3 of 7 dBm.

This work addressed some of the needs of N-Path circuits, such as reduction of the $N \cdot C$ and in-band linearity, this can be further improved by: 1) reducing the power consumption of the clock generation circuit, such as in (PARK; RAZAVI, 2014), 2) implementing solutions to cancel the harmonics of the circuits such as in (XU; ZHU;

KINGET, 2014), improving the LNA to be more robust to capacitance charges and using the circuit to do the mixing such as presented in (PARK; RAZAVI, 2014). The harmonics of the circuit were not cancelled because of the design complexity of a circuit such as in (XU; ZHU; KINGET, 2014), the number of blocks (N-Path filter, LNA, G_m cells) and the power consumption. The LNA from (De Souza; MARIANO; TARIS, 2017) is a great solution for in-band linearity but it was used as a generic block for quick design and proof of concept in this work. By making the LNA more robust to capacitance charges all the parameters of the circuit can be improved. Finally, (PARK; RAZAVI, 2014) uses the N-Path notch filter for both filtering and mixing. This can be done by combining the voltages at baseband ($V_{BB,i}, i = 1, \dots, N$, see figure 5.1a) with the right gain at each path. This was simulated but not fully implemented because of time constraints (see figure 5.1b).

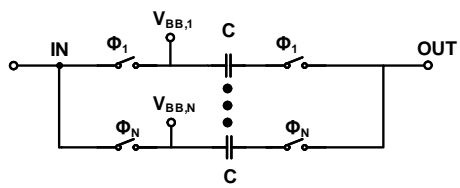
Table 5.1: SoA results of LNAs combined with N-Path filters

	This work	#	*	o
CMOS technology	28 nm FD-SOI	65 nm	65 nm	65 nm
BW_{-3dB} (MHz)	20	20	0.35-20	2.7
Frequency (GHz)	1.0-5.0	0.2 - 1.6	0.05-2.5	0.836-1.88
Gain (dB)	16.5-19	14-24	38	36
Rejection (dB)	26.5	12	24	N.A.
NF (dB)	2.9	3.6	2.9	3.2
In-band IIP3 (dBm)	7	N.A.	-20	-12
Power consumption (mW)	7.2 - 12.2	15.8-20.2	20 @ 2 GHz	20 @ 1.88 GHz

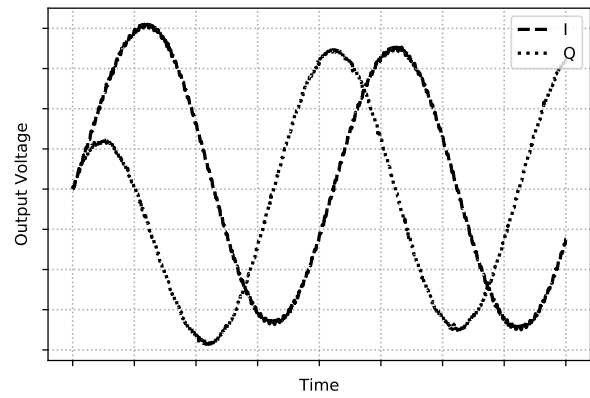
(ZHU; KRISHNASWAMY; KINGET, 2015)

* (PARK; RAZAVI, 2014)

o (QI et al., 2017)



(a)



(b)

Figure 5.1: (a) Baseband voltages used to produce the mixing, (b) simple simulation result using the principle of mixing with no gain.

APPENDIX A

TRANSISTOR SIZING

The transistor sizing for this thesis was mostly determined by the LNA. The best performances for the LNA were obtained by using transistors sized between multiples of 5 or 6 μm . A good practice to layout is break the transistor into multiple fingers. For the 28 nm FD-SOI a good finger width is 1 μm , this decreases the parasitics while enabling quick layout design. The base transistor, replicated in all the designs, was set to 6 μm . So all the circuits designed here were multiples of this base transistor (M transistors in parallel to create a $M \cdot 6 \mu\text{m}$ transistor). Therefore, the inverter cell uses 24 μm transistors (for both P and N), the 3-Input NAND and the D-Latch use 12 μm transistors, with sets and resets at 6 μm . Its also to be noted that the switches used present a higher on-resistance because of this, they are set to 60 μm instead of 63.

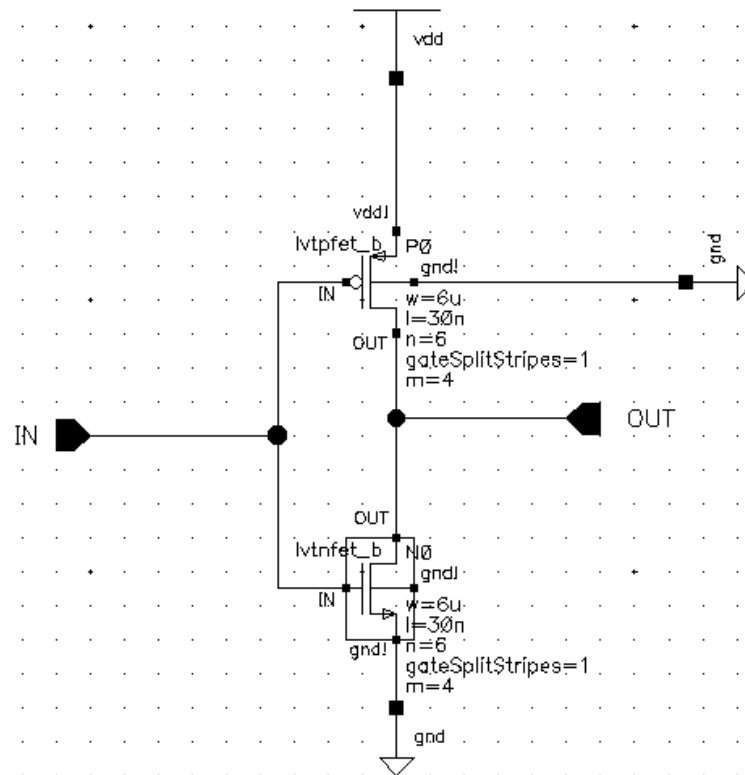


Figure A.1: Virtuoso schematic of the inverter

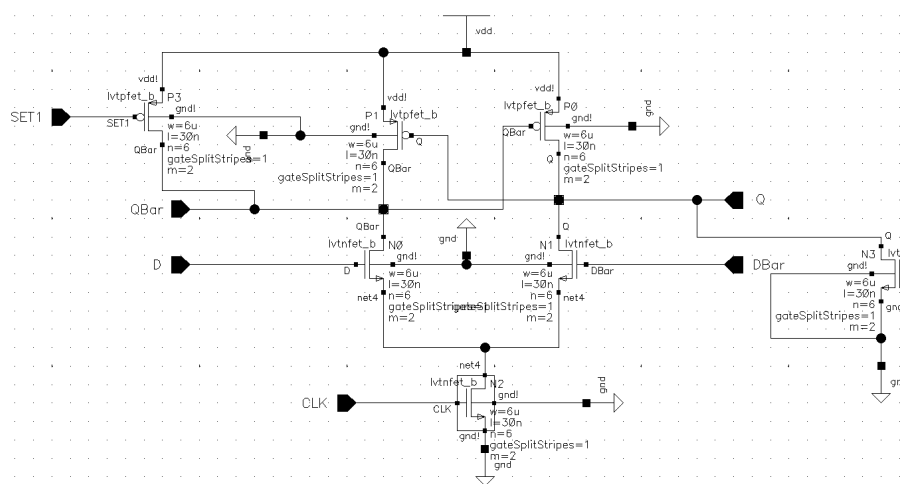


Figure A.2: Virtuoso schematic of the 3-Input NAND

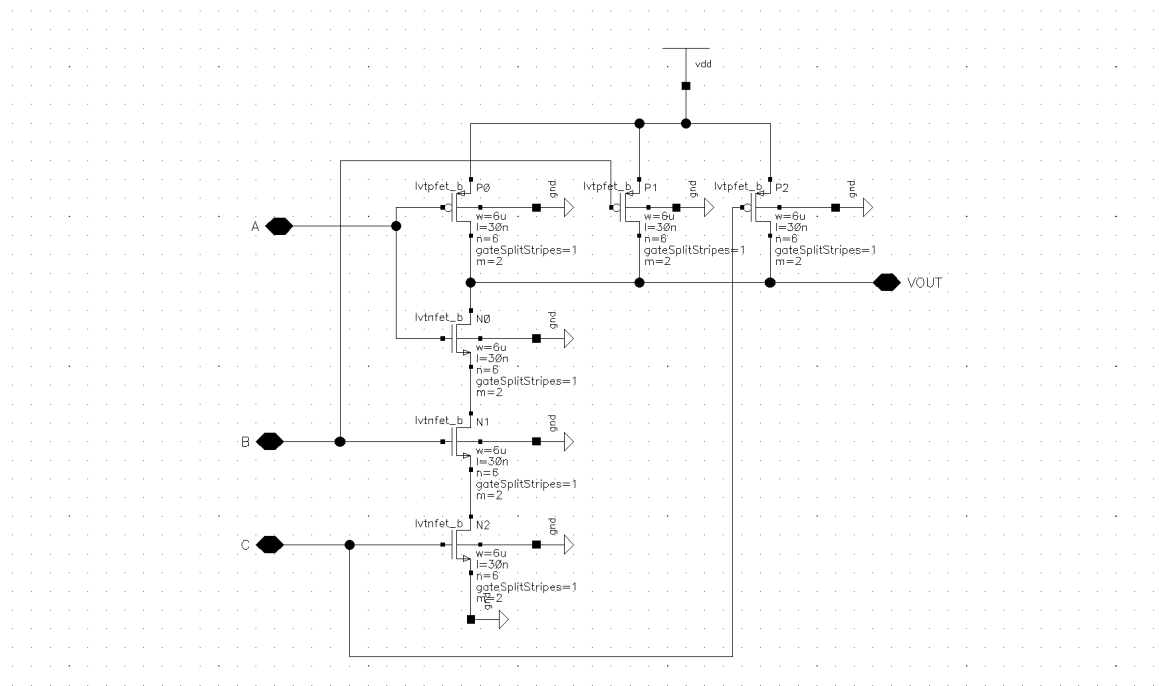


Figure A.3: Virtuoso schematic of the D-Latch

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