UNIVERSIDADE FEDERAL DO PARANÁ

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POWER AMPLIFIER LINEARIZATION METHODS AND IMPLEMENTATION PROPOSITION

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POWER AMPLIFIER LINEARIZATION METHODS AND IMPLEMENTATION PROPOSITION

Trabalho de Conclusão de Curso apresentado ao Programa de Graduação em Engenharia Elétrica, Área de Concentração Circuitos e Sistemas, Departamento de Engenharia Elétrica, Setor de Tecnologia, Universidade Federal do Paraná, como parte das exigências para obtenção do título de Engenheiro Eletricista.

Orientador: Prof. Dr. Luis Henrique Assumpção Lolis

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Trabalho de Conclusão de Curso aprovado como requisito parcial à obtenção do grau de Engenheiro Eletricista no Programa de Graduação em Engenharia Elétrica da Universidade Federal do Paraná, pela seguinte banca examinadora:

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"The edge... There is no honest way to explain it because the only people who really know where it is are the ones who have gone over."
Hunter S. Thompson
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RESUMO

O principal circuito eletrônico de um transmissor de comunicações sem fio é chamado Amplificador de Potência (Power Amplifier PA), este é responsável por comandar uma antena e consome uma grande quantidade de energia. Um grande esforço é feito para conceber um circuito PA que não é somente energeticamente eficiente mas também linear, de modo que o sinal transmitido respeite as restrições da largura de banda do canal de transmissão. Em outras palavras, o PA tem um compromisso entre eficiência espectral e consumo de energia. O objetivo do projeto foi propor uma implementação de linearização de PA em banda base, usando dados facilmente disponíveis, considerando sinais de banda larga. Para isto uma extensa pesquisa bibliográfica na base de artigos do IEEE sobre diferentes métodos de linearização. A pesquisa artigo revelou cerca de 50 artigos sobre métodos de linearização PA apresentando uma ampla variedade de abordagens e resultados. Como resultado a malha Cartesiana (Cartesian Feedback CFB) e pré-distorção digital (Digital Pre-Distortion DPD) mostraram-se como os métodos mais apropriados para esta aplicação. A partir destes dados foi proposto um método baseado em um sistema de feedback cartesiano que atualiza uma 'Look-up-Table' (LUT) que implementa Distorção Pre-Digital. A LUT ocupa uma grande superfície em um circuito integrado, o que aumenta os custos de produção. Por isso outros blocos são adicionados ao sistema, tais como: interpoladores, LUT adaptativa e um regulador adaptativo. Finalmente, é necessário sincronizar os símbolos I/Q de entrada e de feedback para que a LUT seja preenchida corretamente.

Key words: 'Linearization'. 'Cartesian Feedback'. 'Digital Pre-Distortion'.


ABSTRACT

The core electronic circuit of a wireless communication transmitter is called Power Amplifier PA, which is responsible to drive the antenna, consumes a great amount of energy. A big effort is made to conceive a PA circuit that is not only power efficient but also linear, so that the transmitted signal respect the bandwidth constraints. In other words, the PA faces a trade-off between spectral efficiency and power consumption. The project goal was to propose a PA linearization implementation in baseband, using easily available data, considering wideband signals. In the beginning, an extensive article research was performed in the IEEE database of all linearization methods, and as the end of this phase approached more attention was given to Cartesian Feedback and Digital Pre-Distortion methods. The article research revealed about 50 articles about PA linearization methods presenting a broad variety of approaches and results. In the end a proposition method was drawn based on a Cartesian Feedback system updating a Digital Pre-Distortion Look-up-Table. As the LUT occupies a big surface in an integrated circuit, increasing production costs, other blocs are added to the system, such as: interpolators, adaptive LUT and adaptive regulators. Great effort should be taken in order to synchronise input and feedback I/Q symbols so that the LUT is populated properly.

Key words: Linearization. Cartesian Feedback. Digital Pre-Distortion.
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<td>LUT</td>
<td>Look-Up-Table</td>
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<td>PA</td>
<td>Power Amplifier</td>
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<td>PAPR</td>
<td>Peak-to-Average Power Ratio</td>
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<td>Reg</td>
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LIST DE SYMBOLS

θ  Instantaneous vector’s angle
θ'  Estimation of vector’s angle
ϕ  Difference between (θ, θ')
s  Seconds
ms  mili seconds
A  Attenuator
S  Complex signal
I_d  In-phase data symbol
Q_d  Quadrature data symbol
LO  Local oscillator
cos  cossinus
sin  sinus
tan  tangent
L(s)  Feedback’s loop gain
A_n  CORDIC’s gain
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CHAPTER 1

INTRODUCTION

1.1 Context and Motivation

The increasing demand on cheap electronic transceivers, with long battery lifetime, capable of delivering crystal-clear voice, with no lapses in coverage, able to access the internet, motivates researches around the world. A wide variety of fields are contributing with this development, such as, but not limited to: Automation, Circuit Design, Radio Frequency (RF) and Digital Signal Processing (DSP).

The transceiver is a circuit responsible to exchange electromagnetic waves from one device with an antenna or with another device, which is a process that consumes a big share of the circuit’s energy. The Power Amplifier (PA) is the transmitter’s subcircuit, which is responsible to drive the antenna with high-frequency signals, consuming the biggest energy share. A big effort is made to conceive a PA circuit that is not only power efficient but also linear, so that the transmitted signal respect the bandwidth constraints. In other words, the PA faces a trade-off between spectral efficiency and power saving. The former characteristic is necessary if the device needs to meet legal spectrum requirements; the latter, provides long battery life. Nevertheless, there is a solution that can deliver both desirable aspects, which proposes that the PA works in a nonlinear fashion, saving power, and the linearization issue be corrected by some linearization method.

This document is organised as follows: The rest of this chapter discuss briefly about the project’s goals and the state of the art in PA linearization methods. Chapter 2 analyses basic elements of analog and digital Cartesian Feedback (CFB) systems. The digital version of CFB presents some advantages againsts the analog version, neverthe-
less the digital calculation of a vector's phase is usually performed using Look-Up-Table (LUT), which is cumbersome. Chapter 3.1 introduces the CORDIC, which is a small and simple circuit used to calculate a vector's module and phase and to rotate a cartesian vector in a plane. An implementation is proposed in chapter 4 consisting in a Digital Pre-Distortion updated with a CFB feedback. Firstly, previous works who used a similar structure are analysed then an implementation proposition is drawn. Finally, the conclusion in presented in chapter 5.

1.2 Objectives

1.2.1 General objective

The main goal is to perform an introductory work, providing enough information, so that a digital wideband PA linearization integrated circuit can be designed in future works. To accomplish this task specific objectives, presented in the following section, were established to evaluate the performance along the project.

1.2.2 Specific Objectives

State of the art - Research the latest developments in PA linearization techniques

Software Evaluation - Perform simulations and validate system simulation under two different softwares: SystemVUE (Agilent) and Simulink (MathWorks)

Structure Proposition - Propose a digital wideband linearization based on Cartesian Feedback

First Stage Tests - Tradeoff: energy consumption x small circuit surface x fast convergence
1.3 State of the Art of Linearization Methods

One can find in the literature different linearization methods, which can also be combined to improve even further the project’s requirements. These are the most common methods used: Feedback, Feed-forward, Pre-distortion and Post-distortion. Furthermore, even if Envelope Elimination and Restoration (EER) and Envelope Tracking (ET) are methods used to increase the PA’s power efficiency, they were added because they share the same goal i.e. ameliorate overall power consumption.

1.3.1 Feedback

The feedback is based in standard control methods and it is performed in baseband. The output is sampled and compared with the respective input, resulting in an error, which will be treated to maximize linearity. J. Dawson (DAWSON, 2003) gives a great overview of analogical Cartesian feedback systems, which work gave a solid background for CFB development, where a simplified structure can be found in figure 1.1. In this schematic the distorted output is attenuated and down converted so that the errors introduced by the non-linear PA can be subtracted from the input I/Q symbols. The blocs between the mixers and the subtractors are anti-aliasing low-pass filters. Some works introduce the constrains of the digital version, as in (AULERY et al., 2013; SANAA et al., 2012; WRIGHT; DURTLER, 1992), which are discussed latter in this document (section 3). Although CFB is generally suitable for narrowband applications (BRIFFA, 1996), the authors in (JOHANSSON et al., 1993) propose a multi-loop CFB. This system operates using CFB modules (CFBM), with center frequencies across a band.
1.3.2 Feed-forward

The feed-forward method samples an early point to introduce a correction latter on the system. In figure 1.2, the Auxiliary PA serves to invert the Main PA’s frequency response except on the signal’s frequency, which is used to correct the output. Delay blocks are necessary to synchronise both paths. The bulky size combined with the need for good isolators and couplers makes the technique ill-suited for integration (BOO; CHUNG; DAWSON, 2011) but has been popular for base-station applications since it gives a significant linearity improvement for high bandwidth signals.
1.3.3 Pre-Distortion and Post-Distortion

Another linearization method consists in introduce a compensation block before (figure 1.3) or after (figure 1.4) the PA. The main goal is to implement the inverse characteristics of the PA, so the combination of these transfer functions will render a linearized frequency response. The main challenge here is that some circuit parameter, which influences linearity, change over time e.g. power supply, temperature, load charge, etc.

In order to maximize linearity in predistortion systems some authors propose algorithms that are able to update its parameters, such as (PRESTI; KIMBALL; ASBECK, 2012; BOO; CHUNG; DAWSON, 2011; KIM et al., 2010; LI et al., 2009; BOO; CHUNG; DAWSON, 2009; KIM et al., 2008; CHUNG; HOLLOWAY; DAWSON, 2008; GILABERT et al., 2008; ZHI-YONG et al., 2006; WOO; MILLER; KENNEY, 2005; SILLS; SPERLICH, 2002; NORDSJO, 2002; SUNDSTROM; FAULKNER; JOHANSSON, 1996; NAGATA, 1989) Although adaptive methods tend to be time consuming and energy hungry, here adaptation calculations can be done in intervals of $100\text{[ms]}$ or even $1\text{[s]}$. This is possible since the parameters which disturb linearity in time have extreme low frequency contributions. Some authors have also proposed to accelerate the adaptation speed calculations (LI et al., 2009; KWON et al., 2010; CAVERNS, 1990; JEON; CHANG; CHO, 1997; JIN et al., 2003).

Figure 1.3: Pre-Distortion linearization method

Post-distortion linearization methods are not so popular because it tends to waste PA power, which is an expensive resource (TSAI et al., 2007).
### 1.3.4 Envelope Elimination and Restauration

This method consists of firstly separate the signal's phase and amplitude to recombine them latter, as in figure 1.5. The traditional envelope elimination and restoration (EER) system improves the efficiency by driving the radio frequency (RF) transistor in switch mode with a constant amplitude phase signal and superimposing the envelope signal at the collector/drain of RF transistor (WANG et al., 2005; DIET et al., 2004).

![Figure 1.5: Envelope Elimination and Restauration](image)

### 1.3.5 Envelope Tracking

Envelope Tracking (ET), schematically represented in figure 1.6 modulates the principal PA power source so that it can yield maximum linearity (JEONG et al., 2009). Although envelope shaping helps to improve the linearity and overall efficiency of the ET system, it makes the design of the envelope amplifier very challenging since it results in a non-linear and time-varying load to the envelope amplifier. Another challenge is that the timing misalignment is one of the major sources of spectral re-growth in this system (HASSAN et al., 2012b, 2012a; ASBECK et al., 2012; KIMBALL et al., 2008, 2006).
Figure 1.6: Envelope Tracking system
CHAPTER 2

CARTESIAN FEEDBACK

The CFB linearization method present some implementation advantages, such as:

- uses the cartesian coordinates as main information in the linearization process, which information is easily available
- is based on a negative feedback, which tends to generate a stable system
- the linearization is performed in baseband

Analyse the analog CFB system is more intuitive then a digital system, this is why most part of this chapter id dedicated to the analog CFB system. Latter, in this chapter the differences of a digital system are presented.

Figure 2.1 shows a simple CFB block diagram, where: the signals $I_d(s)$ and $Q_d(s)$ are the reference signals; $e_I$ and $e_Q$ are the respective errors signals, which will be
used to analyse the stability, later in section 2.1; \( S \) is the complex signal formed by the added and unconverted \( I \) and \( Q \) signals, which is sent to the antenna; \( I' \) and \( Q' \) are the filtered, demodulated and attenuated by \( A \) signals, used to feedback the system; \( \phi \) is a mathematical representation of a possible delay between the input and output signals and represents the difference of phase between the mixer and the demodulator. and finally; \( H(s) \) is both the loop gain and the dynamics introduced by the linearization strategy.

The main goal of this structure is to take advantage of its stability, the possibility to linearize the system in baseband and the fact that the signals used to implement the correction are easily available with the addition of a down-converter and two Analog-to-Digital (ADC) converters.

### 2.1 Stability analysis

A CFB loop with a nonzero \( \phi \) is said to have phase misalignment which impact can be demonstrated mathematically as follows. Considering that \( S = I \sin(\omega t) + Q \cos(\omega t) \), we see that

\[
I' \approx [I \sin(\omega t) + Q \cos(\omega t)] \sin(\omega t + \phi) \\
Q' \approx [I \sin(\omega t) + Q \cos(\omega t)] \cos(\omega t + \phi)
\]
after using some trigonometric relations, such as

\[2 \sin \alpha \sin \beta = \cos(\alpha - \beta) - \cos(\alpha + \beta)\]  \hspace{1cm} (2.3)

\[2 \sin \alpha \cos \beta = \sin(\alpha + \beta) + \sin(\alpha - \beta)\]  \hspace{1cm} (2.4)

\[2 \cos \alpha \sin \beta = \sin(\alpha + \beta) - \sin(\alpha - \beta)\]  \hspace{1cm} (2.5)

\[2 \cos \alpha \cos \beta = \cos(\alpha - \beta) + \cos(\alpha + \beta)\]  \hspace{1cm} (2.6)

\[\cos(-\alpha) = \cos(\alpha)\]  \hspace{1cm} (2.7)

\[-\sin(-\alpha) = \sin(\alpha)\]  \hspace{1cm} (2.8)

and considering that frequencies from \(2\omega\) will be filtered, we find that

\[I' \approx [I \sin(\omega t) + Q \cos(\omega t)] \sin(\omega t + \phi)\]  \hspace{1cm} (2.9)

\[\approx I \sin(\omega t) \sin(\omega t + \phi) + Q \cos(\omega t) \sin(\omega t + \phi)\]  \hspace{1cm} (2.10)

\[\approx \frac{I}{2} [\cos(\omega t - \omega t - \phi)] + \frac{Q}{2} [-\sin(\omega t - \omega t - \phi)]\]  \hspace{1cm} (2.11)

\[\approx \frac{1}{2} (I \cos \phi + Q \sin \phi)\]  \hspace{1cm} (2.12)

which is applicable to \(Q'\) as well, producing

\[Q' \approx [I \sin(\omega t) + Q \cos(\omega t)] \cos(\omega t + \phi)\]  \hspace{1cm} (2.13)

\[\approx \frac{1}{2} (-I \sin \phi + Q \cos \phi)\]  \hspace{1cm} (2.14)

Ideally, if the phase \(\phi\) is constantly 0 (zero), the CFB should operate as two decoupled feedback loops, one for each component (I and Q). Although, multiple factors contribute to a nonzero \(\phi\), namely delay through Power Amplifier (PA), phase shifts of the RF carrier due to reactive load of the antenna, mismatched interconnect lengths between the local oscillator and the two mixers, slightly changes in temperature, pro-
cess variations, output power and carrier frequency. The equations (2.12) and (2.14) shows that the feedback loops are coupled in a scenario in which \( \phi \) is nonzero.

The stability analysis proposed in (DAWSON, 2003) uses the error signals \( e_I \) and \( e_Q \), which are calculated under certain circumstances:

- The phase misalignment is \( \phi \), represented in figure 2.1
- \( Q_d \) is set to 0 (zero), which is possible due to the consideration that the system is linear
- \( L(s) \) represents de loop gain and the linearised dynamics introduced by the modulator, PA and demodulator.
- \( I = e_I(s)L(s) \)
- \( Q = e_Q(s)L(s) \)

And we obtain

\[
e_I(s) = I_d - (L(s)e_I(s)\cos \phi + L(s)e_Q(s)\sin \phi)
\]  
\[
e_Q(s) = -(-L(s)e_I \sin \phi + L(s)e_Q(s)\cos \phi)
\]

Isolating \( e_Q \) in the equation (2.16) and solving equation (2.15) for \( e_I \), we get, respectively

\[
e_Q(s) = \frac{L(s)e_I(s)\sin \phi}{1 + L(s)\cos \phi}
\]

\[
e_I(s) = \frac{I_d(s)}{1 + L(s)\cos \phi + \frac{|L(s)\sin \phi|^2}{1 + L(s)\cos \phi}}
\]

Before finishing the stability analysis, let’s consider a simple feedback system, shown in figure 2.2, where \( e(s) \) is the error between the input \( X(s) \) and the feedback signal \( Y(s)F(s) \). The output \( Y(s) \) is related to the system through the equation 2.19
\[
\frac{Y(s)}{X(s)} = \frac{H(s)}{1 + H(s)F(s)} \tag{2.19}
\]

now, let's define \( L(s) = H(s)F(s) \) as the loop gain, so that the error signal could be written as

\[
e(s) = \frac{X(s)}{1 + L(s)} \tag{2.20}
\]

Comparing the equations (2.20) and (2.18) we identify the loop transmission of a Cartesian feedback system as

\[
L(s) = L_{CFB}(s, \phi) = L(s) \cos \phi + \frac{|L(s) \sin \phi|^2}{1 + L(s) \cos \phi} \tag{2.21}
\]

Analysing this equation for three different situations

1. \( \phi = 0 \Rightarrow L_{CFB}(s, \phi) = L(s) \)

2. \( \beta \phi = |\frac{\pi}{2}| \Rightarrow L_{CFB}(s, \phi) = L(s)^2 \), worst stable case

3. \( \frac{\pi}{2} < \phi < \frac{3\pi}{2} \), will eventually leads to instability due to the fact that \( \cos \phi > 0 \)

According to (BRIFFA, 1996) the CFB system’s performance is also limited in the demodulation phase as it introduces not only linear errors such as DC offsets, gain and phase imbalance but also nonlinear like inter demodulation distortion. Some works in the literature propose methods to reduce these effects (BATEMAN; HAINES; WILKINSON, 1988), in this report we are considering that they are irrelevant.
2.2 Nonlinear Regulator for Phase Misalignment

The author in (DAWSON, 2003) proposes that an increasing monotonic function, from a misalignment of $\phi = 0$ to $\phi = |\frac{\pi}{2}|$, will be a truly continuous solution to the problem of LO phase alignment, and he presents few arguments of support

- this method does not rely on specific symbols or data pattern
- its realisation is in baseband frequency
- it is easily implemented for does not depend on digital signal processing
- the signals in a CFB are originally analog

![Diagram of phase misalignment](image)

Figure 2.3: Misalignment impact after symbol rotation due to non-linear effects, introduced majorly by the PA

The figure 2.3 represents the phase misalignment on the cartesian plane. The cartesian and polar coordinates are shown for a random symbol at the input of the modulator $(I, Q)(r, \Theta)$. This same symbol is added, amplified, attenuated and then demodulated, in order to be used by the feedback system to correct the system nonlinearities. This symbol, at the output of the demodulator, is also represented in this figure $(I', Q')(r', \Theta')$. The relation between the cartesian and polar coordinates is $I = r \sin \Theta$ and $Q = r \cos \Theta$, where $\Theta$ is its instantaneous phase.
As the signals $I, Q, I'$ and $Q'$ represent enough information about the misalignment and they are available in the system, the monotonic function proposed by the author is

\[
IQ' - QI' = r \sin(\Theta)r' \cos(\Theta') - r \cos(\Theta)r' \sin(\Theta')
\]

(2.22)

\[
= rr'[\sin(\Theta) \cos(\Theta') - \cos(\Theta) \sin(\Theta')]
\]

(2.23)

\[
= \frac{1}{2} rr'[\sin(\Theta + \Theta') + \sin(\Theta - \Theta') - \sin(\Theta + \Theta') + \sin(\Theta - \Theta')]
\]

(2.24)

\[
= rr' \sin(\Theta - \Theta')
\]

(2.25)

\[
= rr' \sin \phi
\]

(2.26)

remembering that the difference of phase between the modulated signal and the de-modulated is $\phi = \Theta - \Theta'$.

Furthermore, as in figure 2.4, the author proposes the addition of two blocks: the first is an amplifier $-G$; the second, is an integrator with its own gain factor $k$. Therefore, the final equation 2.28 is.

\[
\gamma = -kG \int (|r(t)|^2 \sin \phi) dt
\]

(2.28)

![Figure 2.4: Implementation of the phase alignment in the Cartesian feedback system](image)
To understand the effects introduced by these blocks we can firstly consider the phase $\phi$. Although, it is time-dependant, the phenomena responsible for its variation are changes in temperature, process variations, output power and carrier frequency (DAWSON, 2003), all of which can be considered low-frequency disturbances. All in all to express that the phase $\phi$, on output $\alpha$, in figure 2.4, shown in equation 2.27, will tend to introduce slowly changes in the system. Secondly, we can consider the integer not only as a mean filter, eliminating noise and high frequency disturbances, but also as a way to eliminate eventual offsets added in the system (BRIFFA, 1996; DAWSON, 2003; PERRAUD et al., 2004; CHUNG; HOLLOWAY; DAWSON, 2008; KWON et al., 2010; PRESTI; KIMBALL; ASBECK, 2012). At last but not least, the gain $-G$ introduced can be used to tune the loop gain affecting directly the gain and phase margins, rendering the system stable.

The operation of the regulator can be understand as the following: lets consider that in a steady state analysis the difference of phase $\phi = \Theta - \Theta' = 0$, and for any reason, $\phi$ slowly changes to a non-zero value, as previously explained; then, in figure 2.4, $\alpha = rr' \sin \phi$ will also change, but as $\phi$ is small we can consider that $\sin \phi \approx \phi$; furthermore, after a few samples, $\gamma$ will output a mean value of these changes, all multiplied by a factor $-G$; finally this averaged multiplied angle will serve as an input to apply a rotation in $I$ and $Q$ in order to correct the phase misalignment. Lets say that the modules of $r$ and $r'$ are held constant,

$$\Theta = \frac{\pi}{4}, \quad \Theta' = 0 \quad \rightarrow \quad \phi = \frac{\pi}{4} \quad \rightarrow \quad \hat{\phi} = -kGr'r' \int_{t_0}^{t_1} \frac{\pi}{4} dt \quad (2.29)$$

in this case, the correction $\hat{\phi}$ sent to the symbol rotator block is negative, reducing the angle of $S$ from $\frac{\pi}{4}$ closer to 0. In this case we will reduce the difference between the angles $\Theta$ and $\Theta'$.

There are basically two methods of implementing the phase shift compensation $\phi$ in the CFB system: the first consists in rotating the baseband symbol, while the
other lies in changing the local oscillator’s phase. In (DAWSON, 2003) the author comments about the power efficiency of the former over the latter. The symbol rotation is implemented by the block with inputs $I$, $Q$ and $\Theta$, in figure 2.4.

### 2.3 Mixed CFB

A digital linearization technique, in contrast to the analog form, means that the modulator, PA and demodulator are still analog, and at least one of the other components (filters, regulators, phase correctors and LUT) are digital. So, as one part of the loop will still be analog while the other will be digital, then two conversions steps will be added to the loop, allowing the communication between the digital and analog blocs.

In one hand the digital version introduces latency due to phase calculation, analog-to-digital conversion (ADC), digital-to-analog conversion (DAC); on the other, digital signal processing increases the robustness of the system (GIMENO-MARTIN; PARDO-MARTIN; ORTEGA-GONZALEZ, 2010). these are some other advantages in the digital implementation

- the nonlinearity introduced by the regulator in section 2.2 will not appear in the digital implementation.
- digital data is robust against noise
- a pre-distortion system can be implemented so the overall transfer function system tends to be unitary
- Feedback and Digital Pre-Distortion are usually combined in other to increase bandwidth
- DSP techniques allow wideband applications

On radio systems some elements like mixers, combiners and PA are still analog. Combining the advantages in both fields to develop a Cartesian Feedback system
yields a Mixed CFB, which basic structure can be seen in figure 2.5.

Figure 2.5: Simplified schematic of a mixed CFB system

From the filters to the antenna the circuit remains analog whereas the regulation part is done digitally. Digital-to-Analog (DAC) converters are added in the transmission and Analog-to-Digital (ADC) converters are placed in the feedback path. These converters add latency to the system which needs to be precisely controlled so that the error calculation subtracts the corresponding symbols. This is why a delay block needs to be added to the circuit. The last modifications introduced in this figure are the Cordic vectoring and Cordic rotation. The former calculates a cartesian vector’s phase and module; the later, rotates a cartesian vector of a given angle. In other words, a CORDIC is the name of a specific circuit capable of calculate the module and phase of a vector, given its cartesian coordinates (Cordic vectoring) and change the angle of a vector given its cartesian coordinates (Cordic rotation). These operations could be performed using Look-Up-Tables (LUT), but they consume great circuit surface, while a CORDIC can be implemented using only shift and add operations in a recursive manner. Next chapter explains this circuit in detail.
CHAPTER 3

CORDIC

One of the problems to be solved in a digital CFB system implementation is the conversion of cartesian-polar-cartesian coordinates. For this purpose a Look-up-Table (LUT) can be used, but memory space and interpolation methods cost both circuit space and energy. An alternative to solve this issue is a method called CORDIC, which will be explored in the next section.

3.1 CORDIC

A COrdinate Rotation Digital Computer (CORDIC) it is a class of shift-add algorithms for rotating vectors in a plane. Its adaptive algorithm performs rectangular to polar conversions as well as rotate vectors in a plane. This algorithm, as we are going to see, is an excellent alternative to convert cartesian and polar coordinates, of a vector in a plane, using digital components as adders, subtractors and shifters. These components are easily available and do not consume great amount of power. This algorithm, developed in (VOLDER, 1959; ANDRAKA, 1998), is derived from the general rotation transform:

\[
\begin{align*}
    x' &= x \cos \phi - y \sin \phi \\
    y' &= y \cos \phi + x \sin \phi
\end{align*}
\]  

(3.1)

which can be rearranged, so that
\[
\begin{align*}
  x' &= \cos \phi [x - y \tan \phi] \\
  y' &= \cos \phi [y + x \tan \phi]
\end{align*}
\] (3.2)

next, we if we consider only the angles, in which \(\tan(\phi) = \pm 2^{-i}\), the multiplication is resumed by a simple shift operation and it suffices to add \(d = \pm 1\) depending on the rotations direction. Considering also that at each iteration, \(\cos(\delta_i) = \cos(-\delta_i)\), independently of the direction, the iterative rotation can be rewritten as

\[
\begin{align*}
  x_{i+1} &= K_i [x_i - y_i d_i/2^i] \\
  y_{i+1} &= K_i [y_i + x_i d_i/2^i]
\end{align*}
\] (3.3)

where \(K_i\) replaces \(\cos \phi\), which can be derived from,

\[
\begin{align*}
  \cos^2 \phi + \sin^2 \phi &= 1 \quad \rightarrow \quad \cos^2 \phi = \frac{1}{1 + \tan^2 \phi} \\
  \text{where } \phi &= \tan^{-1}(2^{-i}) \quad \rightarrow \quad \cos(\tan^{-1}(2^{-i})) = \frac{1}{\sqrt{1 + \tan^2(\tan^{-1}(2^{-i}))}} \\
  \rightarrow \quad \cos(\tan^{-1}(2^{-i})) &= \frac{1}{\sqrt{1 + (2^{-i})^2}} \quad \rightarrow \quad (3.5) \\
  \rightarrow \quad K_i &= \cos(\tan^{-1}(2^{-i})) = \frac{1}{\sqrt{1 + 2^{-2i}}} \quad (3.7)
\end{align*}
\]

Separating the scale constant \((K_i)\) of the equation, the calculation becomes easy being performed only by shift-add operations. The gain after \(n\) iterations \((A_n)\), can be calculated as

\[
A_n = \prod_{i=0}^{n} K_i = \prod_{i=0}^{n} \sqrt{1 + 2^{-2i}} \quad (3.8)
\]
Moreover, another equation, adder-subtractor accumulator, can be added in order to calculate the vector's rotation.

\[ z_{i+1} = z_i - d_i \tan^{-1}(2^{-i}) \]  

(3.9)

The CORDIC operates in one of two modes: rotation (section 3.1.1), rotating an input vector by a specific angle; vectoring (section 3.1.2), rotates the input vector to the x axis while recording the angle required to make that rotation. Both modes uses the same set of equations 3.1.

\[
\begin{align*}
x_{i+1} &= x_i - d_i y_i 2^{-i} \\
y_{i+1} &= y_i + d_i x_i 2^{-i} \\
z_{i+1} &= z_i - d_i \tan^{-1}(2^{-i}) \\
A_n &= \prod_n \sqrt{1 + 2^{-2i}}
\end{align*}
\]

(3.10)

3.1.1 CORDIC Rotation

This method rotates a vector in a plane. The initial conditions are: \( x_0 = X, \ y_0 = Y \) and \( z_0 = \alpha \), where \( d = -1 \) if \( z_i < 0, +1 \) otherwise. This method provides the following results after n iterations:
\[ x_n = A_n [x_0 \cos z_0 - y_0 \sin z_0] \quad (3.11) \]
\[ y_n = A_n [y_0 \cos z_0 + x_0 \sin z_0] \quad (3.12) \]
\[ z_n = 0 \quad (3.13) \]
\[ z_n = 0 \quad (3.14) \]

Lets say we want to rotate the green vector positioned in \textit{polar}(1, \pi/4) of about \pi/8 degrees. We can see in figure 3.1 the green and red vectors representing, respectively, the starting and resulting vectors. The iterations for \(x_i\) and \(y_i\) in equation 3.1 are implemented, resulting in the blue vectors marked \(i \!=\! n\). We can see also dashed lines that shows the progress of the algorithm. these are some of the conclusions that we can draw about this implementation:

- at the first iteration the green unitary vector is moved to position \(i \!=\! 0\), with coordinates \textit{polar}(1, \pi/2)
- in the course of the iterations we see that the vector is moved from its current position towards its desired position (red vector).

\[ \begin{align*}
y
\end{align*} \]

\[ \begin{align*}
0
\end{align*} \]

\[ \begin{align*}
x
\end{align*} \]

Figure 3.1: A CORDIC’s implementation in rotation mode
• we notice that the angle of the blue vectors converges to the red vector’s angle

• from the second iteration \((i = 1)\) we notice that its module changes, outstripping
  the unitary circle. This is due to the \(K\) factor, explained in equation 3.7, which is
  going to be taken into account shortly

The calculation of these new coordinates introduce an amplification on the vector
through the iterations equals to \(A_n\), according to equation 3.1. So, in order to recover
the unitary cartesian coordinates, or the \(\sin\) and \(\cos\) values, the factor \(A_n\) should be
devised the new coordinates.

For the sake of visualisation we consider in this example only 4 iterations, but in
general the number of iteration represents a tradeoff between minimize error and and
maximize speed.

\subsection{3.1.2 CORDIC Vectoring}

This method calculate the angle and module of a vector in a plane. The initial conditions
are: \(x_0 = X\), \(y_0 = Y\) and \(z_0 = 0\), where \(d = +1\) if \(y_i < 0\), \(-1\) otherwise. This method
provides the final results after \(n\) iterations:

\begin{align*}
x_n &= A_n \sqrt{x_0^2 + y_0^2} \\
y_n &= 0 \\
z_n &= z_0 + \tan^{-1}(y_0/x_0)
\end{align*}

There is no sense in represent the new coordinates in a plane, as we did in section
3.1.1. Here, \(x_n\) calculates de module of the initial vector, multiplied by the factor \(A_n\).
And \(z\) calculates its angle in the plane.
3.2 CORDIC Implementation

these are some reasons why this algorithm is used to retrieve the angle of a vector and to rotate it

- the angles \( \phi = \tan^{-1}(2^{-1}) \) are constants
- the operations \( 1/2^{-i} \) are realised by shift operations
- \( \lim_{n \to \infty} K_i \) converges to 0.6073 and \( \lim_{n \to \infty} A_n \) converges to 1.647 (ANDRAKA, 1998)
- The operations are done only by add and shift operations, with no need of divisions or multiplications
- The number of iterations will determine the result’s precision

In next sections difference architectures are going to be analysed

The work in (ANDRAKA, 1998) is considered a cornerstone in CORDIC implementation, so we are going to use its definition to classify the different architectures in the next sections.

3.2.1 CORDIC Iterative Design

The design is generally implemented in a FPGA, allowing to perform digital calculations in a parallel fashion. The parallel data paths, on the other hand, do not map well in FPGA because of the high fan-in required, and this kind of implementation requires several layers of logic. The result is a design that uses a large number of logic. A considerably more compact design, using serial arithmetic, works at a much higher clock rate than its equivalent in parallel design. Although the serial can operates near the maximum toggle frequency of the FPGA, it needs \( w \) cycles to perform each iteration (\( w \) is the data length and the precision of the system). Despite the biggest area used
in parallel applications its speed is yet better than its equivalent in a serial dewing. So, major tradeoff to consider when implementing a CORDIC is area versus speed (ANDRAKA, 1998).

This kind of processor design implements the equation structures, as in equation 3.1, in a recursive fashion. The author in (ANDRAKA, 1998) presents two basics structures, parallel and serial data paths, commenting about their basic advantages and disadvantages.

3.2.2 CORDIC On-Line Design

This implementation is about unroll the recursive operations from section 3.2.1, so that some repetitive operations could be simplified, which results in two major advantages:

- Each iteration \( n \) will implement a word shift, and the shift is always the same for a given iteration \( (n = 0 \rightarrow \gg 0; n = 1 \rightarrow \gg 1; \ldots) \)

- The angle’s value for each iteration is constant, so they can be hardwired across the CORDIC instead of being stored.

By doing such modifications the circuit becomes strictly combinational, depending in nothing but adder-subtractor blocs. And even if this modus operandi is faster than its iterative equivalent, pipeline registers can be implemented to increase even more its speed.
CHAPTER 4

CFB IMPLEMENTATION

The project’s main specifications to the conception of a PA linearization scheme are:

1. Use cartesian feedback as the basic structure taking advantage not only of pre-existent information (I/Q signals) but also of the intrinsic stabilisation provided by feedback systems

2. Implement a digital linearization

3. Linearize PA for Long Term Evolution (LTE) applications, requiring 20MHz of bandwidth

4. Solve the trade-off in order to best respond to: low energy consumption, small circuit space and fast convergence

The first two items lead directly to a Digital Cartesian Feeback (DCFB) implementation. As seen in section 3 the digital implementation of a digital PA linearization has some advantages against its analog counterpart. Although, it introduces latency to the system through the ADC and DAC converters, which bottlenecks the signal’s bandwidth. To solve this problem numerous authors (LIANG; CHEN; CHEN, 2014; PRESTI; KIMBALL; ASBECK, 2012; BOO; CHUNG; DAWSON, 2011; CHUNG; HOLLOWAY; DAWSON, 2008; GILABERT et al., 2008; WOO et al., 2007) have introduced a Digital Pre-Distortion (DPD) block to the design, using a LUT, which can solve the bandwidth constrain and the third specification. In the other hand, DPD demands circuit space to implement the LUT, it adds circuitry complexity and increase energy consumption, depending on how it is implemented. Some authors are using different techniques to ease these negative effects, which will be seen in section 4.1, and can provide good so-
olution for specification number 4. Another crucial consideration that must be taken into account in DPD systems is the synchronisation between the input and output signals.

To sum up, the linearisation method proposed is a modified Digital Pre-Distortion updated by a Digital Cartesian Feedback (DPD-DCFB) that is able to converge quickly, with a small energy consumption that occupies a small surface area.

4.1 CFB-DPD State of the Art

In the following section we are going to present some DPD-DCFB state of the art techniques and introduce some ideas, which can be used in our implementation.

4.1.1 Presti

Figure 4.1 represents the simplified block diagram presented by (PRESTI; KIMBALL; ASBECK, 2012), in which they use a CFB to feed a DPD LUT. According to the authors, the pre-distorted complex envelope \(V_{pd}\) is calculated by multiplying the input complex envelope \(V_i\) by a complex number \(F\). This complex factor \(F\) is majorly a function of the input's amplitude, as the PA distortion is a function of the amplitude signal. This is why the DPD LUT can have 1D (input amplitude). The DPD system implemented in this design is managed by two blocks: the input loop delay and the predistortion LUT. According to (CAVERS, 1990), the input magnitude is an optimal way to reference the LUT, which is the method used by this and most other authors using DPD.

The authors emphasises the choice of using a digital Intermediate Frequency (IF): it ideally eliminates the problems of dc offset, impairments, and low-frequency noise that would affect an analog direct-conversion receiver. It also allow the use of only one ADC decreasing the circuit space and power consumption. In the second down-conversion block, which is digital, the authors use a frequency \(f_{ck}/4\) so the numeric oscillator signals degenerate to \(\cos(n\pi/2) = 1, 0, -1, 0, ... -\sin(n\pi/2) = 0, -1, 0, 1, ...\).
As a consequence the down-converter is simplified to negation and multiplexing, decreasing even further its power consumption and circuit space.

In order to decrease quantisation error the number of entries in the LUT should increase (CHUNG; HOLLOWAY; DAWSON, 2007), the drawback is an augmentation in time convergence (LIANG; CHEN; CHEN, 2014) and space. In this article a 64 position LUT is proposed, which is simplified to one single position during adaptation phase. A mean linearisation value is calculated for all input amplitudes and attributed to all 64 positions equally. After some iterations all 64 positions are enabled to update independently in a DPD fashion. Figure 4.2 shows both phases, respectively, Automatic Gain Control (AGC) and DPD attribution. This method speeds convergence speed due to the fact that some amplitudes have a bigger occurrence probability.

4.1.2 Liang

Figure 4.3 is a diagram block representation of the linearisation implementation in (LIANG; CHEN; CHEN, 2014).

This author’s main concern is the adaptation speed, to this end a quadratic inter-
interpolation is proposed along with a LMS adaptive algorithm. Once LUT has converged the RF feedback path and LUT update are powered down to decrease power dissipation. The author states that linear interpolation improves the linearisation over a simple LUT, but better results can be achieved using a quadratic interpolation. This interpolation method not only remains easy to implement but also provides a fast convergence consuming less circuit space, due to the fact that less LUT entries are required.
4.1.3 Li

Next figure is a block diagram representing the linearisation implemented in (LI et al., 2009).

Figure 4.4 shows the DPD system used in (LI et al., 2009), which consists basically on two adaptive blocks: a multilevel LUT and a loop delay. The multilevel LUT is composed by $N = (0 : 6)$ layers of $2^N$ LUTs, which are updated by a Least Mean Square (LMS) algorithm. This system requires the size of almost 2 times $2^N$ position LUT ($2 \times 2^6 = 128$), but it yields an adaptation 9 times faster than its equivalent 64 position LUT.

The loop delay estimation is done in two steps: Integer delay, which is based in the intercorrelation function; Fractional loop delay, based in a 4-tap interpolated Farrow FIR filters.
4.2 Proposition

In this section a DPD-DCFB linearization system is proposed (figure 4.5) to be simulated and implemented in two phases. First phase, consists of a basic linearisation system can be validated, verifying Adjacent Channel Power Ratio (ACPR) reduction. Second phase, different modifications can be added to improve linearisation performance according to the project's constrains.

Blocks to be implemented on the first phase of linearisation

I/Q symbols - The symbols can be obtained by using a QPSK modulation

Synchronization (Sync) - Forward and feedback paths need to be synchronised before regulation due to the use of filters and converters in the system. Synchronisation can be fixed
Regulator (Reg) - Initially the regulator can consists of a simple subtraction as $I_r = I_s - I'$

Look-up-Table (LUT) - A 64 LUT provides a good trade of between quantisation error and conversion time. Indexing can be performed using input amplitude’s module ($I_d/Q_d$ and $I_s/Q_s$) for read and write, respectively.

Interpolation (Interpol) - A linear interpolation can be used in a first linearisation step

Power Amplifier (PA) - Create a block capable to represent the PA’s distortions. The PA have 2 non-linear characteristics contributions: static and dynamic. The former is represented from equation 4.1 to 4.3. Furthermore, its magnitude and phase can be modelled as equations 4.2 and 4.3 (SALEH, 1981). And the latter consists of memory effects, which causes the output to be dependent not only on the input but also on its previous state. In a first moment we are not interested in a dynamic PA.
\[ G(r) = K(r)e^{\Phi(r)} \]  
\[ K(r) = \frac{a_ar}{1 + \beta_ar^2} \]  
\[ \Phi(r) = \frac{a_pr^2}{1 + \beta_pr^2} \]

\( K(r) \) and \( \Phi(r) \) are the PA’s AM-AM and AM-PM, static characteristics, respectively. The parameters \( a_a = 2.2, \beta_a = 0.23, a_p = -4.033, \beta_p = 9.104 \) where used to model a PA with negligible memory effects in (LIANG; CHEN; CHEN, 2014), and \( r \) is the normalised signal amplitude.

**Attenuator (Att)** - The goal is to subtract the power added at the PA

**Mixer** - According to (LIANG; CHEN; CHEN, 2014) simulation can be performed in baseband, so in this phase \( f_{\text{carrier}} \) can be set to 0[Hz].

In a second phase of linearisation simulation some parameters will be taken into account as: circuit space, conversion speed and computational cost.

- Generate a symbol sequence based on LTE signals (QPSK, 16QAM and 64 QAM)
- Redesign diagram blocks to take into account the circuit delays (CORDIC)
- Introduce adaptive fractional synchronisation between forward and feedback signals
- Propose a regulator capable of provide a faster convergence
- Propose an adaptive LUT to increase even further convergence speed and decrease circuit space implementation
- Implement different orders and methods of interpolation aiming conversion speed and energy consumption
• Approach the PA’s model to component simulation values
• Introduce mixer and conversion (ADC / DAC) non-linearities
CHAPTER 5

CONCLUSION

With the considerable increase of electromagnetic communication systems and protocols, modern standards demand highly complex schemes to provide spectrally efficient solutions. These complex modulations have, in most cases, non constant envelopes which needs to be amplified linearly. Often these modulations have high Peak-to-Average Power Ratios (PAPR) and require a linear signal amplification leading to low PA power efficiency. Recent modulation techniques also uses sideband signals, like LTE 20MHz bandwidth.

As various linearisation methods have been proposed in the literature, this work focused on present a general overview of these studies and propose a few guidelines for a future simulation, implementation and circuit conception. Some considerations were taken to propose a linearisation method for a wideband LTE signal as energy efficient, small circuit space and fast convergence.

A DCFB is a good choice considering a handset application and only depends on coded symbols (I/Q) and the addition of a downconverter. A DPD block in one hand enables large bandwidth applications, on the other, degenerates circuit space and conversion time. Nevertheless, these drawbacks can be corrected by some manipulations on how the LUT is populated and how the input signal is corrected.

A two step simulation is proposed: Firstly, a simplified linearisation can be performed using only the digital part of figure 4.5; Secondly, some modifications can improve the overall system performance and precision.

Two softwares were evaluated to implement the whole simulation: SystemVUE (Agilent) and Simulink / Matlab (Mathworks). The former in one hand performs time and
frequency simulation altogether, on the other, lacks on manual pages and explanation of function parameters; the latter, provides a good solution given that simulation can be performed in baseband and previous experience will speed phase.


BRIFFA, M. A. Linearization of RF Power Amplifiers. Tese (Doutorado) — Victoria University of Technology, Melbourne VIC 8001, Dec 1996.


